Inverse-Designed Mode-Encoded Photonic Logic Gates With Reference-Light-Free Operation

Chihyeon Kim, Jaehyun Hong, Ik Ju Kim, Jinwoong Cha, and Haejun Chung

(Invited Paper)

***Abstract*—Optical logic gates offer a promising route toward high-speed, energy-efficient photonic computing. Still, conventional intensity-encoded architectures often require a reference or bias light to implement nontrivial Boolean functions such as NAND and NOR. Here, we propose an inverse-designed optical logic gate that encodes binary information in guided spatial modes rather than optical intensity. In the proposed scheme, the logical states "0" and "1" are represented by the TE_{00} and TE_{10} modes of a multimode silicon waveguide, enabling both logic states to carry optical power and eliminating the need for an external reference beam. Using full three-dimensional adjoint-based topology optimization, we design six two-input, single-output Boolean gates on a silicon-on-insulator platform, including AND, OR, XOR, NAND, NOR, and NXOR, within $4 \times 4\,\mu m^2$ footprint. The optimized devices realize the target truth-table behavior by selectively transmitting the desired optical modes while suppressing unwanted mode crosstalk, ensuring that each input combination yields the correct logical output (0,1) for the corresponding optical modes (TE_{00}, TE_{10}). The XOR gate maintains a signal-to-noise ratio(SNR) above 5 dB across the 1.5–1.6 μm wavelength band despite being optimized only at 1.55 μm, owing to distributed multimode interference rather than narrowband resonance. We also show that the same physical structure can switch between XOR and NXOR operations by tuning only the relative phase between the two input signals. These results demonstrate compact, broadband, and reconfigurable mode-encoded Boolean logic elements while identifying the power and phase requirements that must be addressed for their extension toward multistage photonic circuits.**

***Index Terms*—Adjoint optimization, inverse design, optical computing, optical logic gates, silicon-on-insulator (SOI).**

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I. Introduction

THE rapid growth of artificial intelligence and cloud computing has increased the demand for computing systems with higher throughput, lower latency, and improved energy efficiency. Optical computing has attracted considerable interest because light offers high bandwidth, low propagation latency, and multiple degrees of freedom for information processing [1], [2], [3], [4], [5], [6], [7]. However, optical computing encompasses several distinct computational approaches that should be distinguished according to the form of information being processed and the intended computational task.

Diffractive optical processors, optical neural networks, and computational-imaging systems generally operate on continuous optical fields. These systems exploit diffraction, interference, or trained optical transformations to perform operations such as matrix multiplication, inference, and image processing [2], [5], [6]. Such analog or neural optical approaches are conceptually distinct from digital optical logic, in which information is represented by discrete logical states and processed according to Boolean functions. The present work focuses on the latter. Specifically, we investigate device-level combinational Boolean logic in which two binary inputs are transformed into a discrete binary output encoded in guided optical modes.

Optical Boolean gates have been investigated using a variety of device configurations. Mach–Zehnder interferometers implement logic functions by controlling the relative optical phase between two propagation paths [8], [9], [10]. Micro-ring-resonator approaches have employed wavelength-selective resonance, active tuning, nonlinear effects, and polarization or mode conversion [11], [12], [13], [14], [15], [16]. Optical Boolean logic has also been investigated using photonic-crystal structures [17], [18], plasmonic circuits [19], and nonlinear optical devices with signal restoration or gain [20]. These implementations differ

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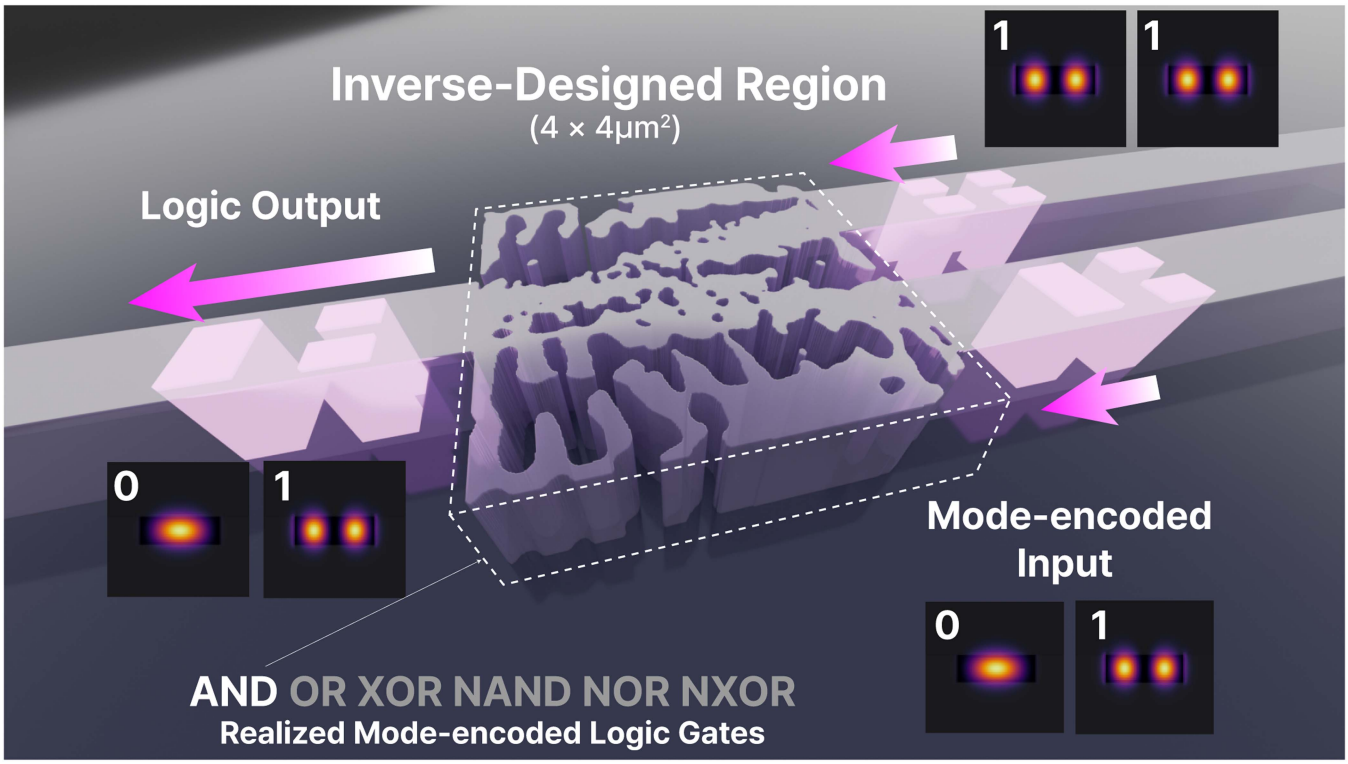

Fig. 1. Concept of an inverse-designed mode-encoded optical logic gate. Two input bits are encoded into distinct guided modes, where the logic states "0" and "1" correspond to different modal field profiles. The mode-encoded inputs propagate into a compact inverse-designed region with a footprint of $4 \times 4\,\mu\mathrm{m}^2$, where the optimized permittivity distribution transforms the input mode combination into the desired output state. The logic result is decoded from the output modal profile, enabling the realization of Boolean logic functions such as AND, OR, XOR, NAND, NOR, and NXOR within the same inverse-design framework.

in their footprint, bandwidth, encoding method, optical power requirements, phase sensitivity, and suitability for multistage operation.

Beyond the choice of a particular interferometric, resonant, or nonlinear device configuration, inverse-design methods provide another route for realizing compact photonic devices with tailored optical responses. Rather than restricting the design to a small set of predefined geometric parameters, inverse design explores a high-dimensional spatial design space and can identify non-intuitive permittivity distributions that achieve a prescribed optical function. These methods have been implemented using deep learning [21], [22], [23], [24], global optimization [25], [26], [27], [28], and adjoint-based topology optimization [29], [30], [31].

Among these approaches, adjoint-based topology optimization is particularly well suited to photonic problems involving a large number of design variables. For a given excitation and scalar objective, one forward and one adjoint electromagnetic simulation provide the gradient of the objective with respect to all design variables. By combining the forward electromagnetic response with an adjoint field derived from Lorentz reciprocity, the adjoint method determines how local permittivity perturbations affect the prescribed optical response [30]. This capability has enabled the design of compact devices with complex optical functions, including wavelength routing, mode conversion, and other tailored electromagnetic responses [29], [32], [33], [34]. Inverse-design methods have also been applied to optical Boolean logic, yielding devices with compact footprints and tailored transmission characteristics [35], [36], [37], [38], [39].

Building on this approach, we design inverse-designed logic gates that operate on optical mode-encoded signals as shown in Fig. 1. Despite advances in optimization techniques, most optical logic gates, including many inverse-designed implementations, still encode binary information using optical intensity, where the logic states "0" and "1" correspond to the absence and presence of light, respectively [8], [9], [10], [11], [12], [13], [25], [26], [27], [35], [36], [37], [38], [39], [40]. This intensity-encoding scheme creates a fundamental challenge for logic gates such as NAND, whose truth table requires a high output for the all-zero input state, as shown in Fig. 2. Because the (0, 0) input carries no signal light, a passive intensity-encoded device cannot generate the required logical "1" output from the input signals alone. Such architectures, therefore, typically require an additional reference input, or an active/nonlinear mechanism, to supply the output optical power. This additional component increases the complexity of the optical routing and control architecture and requires an alternative strategy to enhance the scalability of optical logic devices.

To address this challenge, we propose to encode binary information in the spatial modes of a guided wave rather than in optical intensity. In this scheme, the logic states "0" and "1" correspond to distinct guided modes, TE_{00} and TE_{10}, so both binary states carry optical power. A related concept has been explored in logic gates based on micro-ring resonators that exploit TE and TM modes [14]. Here, we implement this mode-encoding scheme in compact, inverse-designed multimode interferometers. Unlike micro-ring resonators, the proposed device does not rely on narrowband optical resonance;

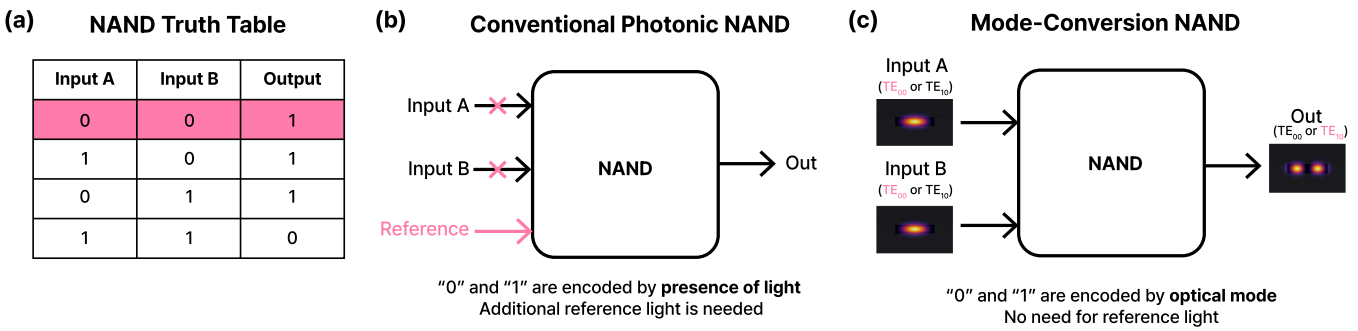

Fig. 2. Operating principle of the mode-encoded photonic NAND gate. (a) NAND truth table. (b) Conventional intensity-encoded photonic NAND gates represent "0" and "1" by the absence and presence of light, respectively. Therefore, the "00" input case requires an additional reference or bias light to produce the logical output "1". (c) The proposed mode-encoded NAND gate represents binary states using distinct guided modes, such as TE_{00} and TE_{10}. Because both logic states carry optical power, the NAND operation can be realized through mode conversion without an additional reference light.

instead, it performs logic operations through distributed multi-mode interference and mode conversion. This nonresonant operating mechanism provides three key advantages over conventional intensity-encoded or resonance-based architectures: (i) reference-light-free operation enabled by mode encoding, (ii) broadband response across a wavelength range of approximately 100 nm, and (iii) phase-controlled reconfigurability between different logic functions within the same physical structure.

We realize this concept by designing a free-form multi-mode interference region that controls the interference and conversion of input spatial modes. We optimize the device using an adjoint-based topology optimization framework, which efficiently searches the design space for a permittivity distribution that maps each input-mode combination to the desired output mode. To ensure fabrication feasibility, we impose minimum feature-size constraints during optimization, yielding Silicon-on-insulator (SOI)-compatible patterns that can be fabricated with standard lithography. Fig. 1 shows a schematic of the proposed mode-encoded optical logic device.

The present study concerns individual combinational logic elements and does not constitute a complete von Neumann optical computer. The present devices rely on coherent interference, and their operation depends on the relative phase of the input fields. Their target-mode transmission also remains below unity. We therefore examine the requirements for multistage operation by analyzing the optical power budget, input-phase sensitivity, output-phase response, linear-scattering constraints, and phase-constrained inverse design. These analyses identify the power and phase conditions that must be addressed before arbitrary cascading of independently optimized gates can be achieved.

This paper is organized as follows. Section II describes the device geometry and optimization procedure, including the rationale for using full three-dimensional electromagnetic simulations rather than a two-dimensional approximation. It also covers the adjoint-based optimization framework and fabrication-aware constraints. In Section III, we demonstrate the reference light-free truth-table operation of the six logic gates and characterize the responses of individual devices, including their broadband operation and variations with etch bias and relative input phase. Phase-controlled reconfigurability is also demonstrated, with particular emphasis on the XOR gate. We further examine the feasibility of cascading the mode-encoded logic gates from multiple perspectives, including power efficiency, input- and output-phase responses, linear-scattering constraints, and phase-constrained inverse design. Overall, we established an adjoint-optimized framework for mode-encoded optical logic gates and identified the system-level considerations required for their extension from individual devices toward more complex photonic computing circuits.

II. Methods

A. Optimization Methods

We perform all simulations and optimizations using Meep [41], an open-source full three-dimensional finite-difference time-domain (FDTD) solver. Most inverse-designed PICs use 2D simulations to reduce the substantial computational cost associated with full 3D analysis. A common approximation is the effective-index method [42], which first estimates the vertical confinement of the slab mode in the out-of-plane (z) direction and then solves the in-plane propagation problem using an effective refractive index. However, this approximation becomes inadequate for the proposed device because the logic gates operate through interference and conversion between spatial modes in a 220-nm-thick SOI waveguide. In particular, the effective-index method does not accurately reproduce the vectorial field profiles and modal overlap of higher-order guided modes, as shown in Supporting Section S1 Fig. S1. We therefore adopt full 3D FDTD simulations throughout the optimization to capture the mode profiles, vertical confinement, and multi-mode interference with sufficient accuracy.

The simulations use a 220-nm-thick SOI platform with an air upper cladding. This configuration does not require an additional oxide overcladding deposition step, thereby simplifying the fabrication process. The simulation structure consists, along the out-of-plane (z) direction, of a 1 μm SiO_2 bottom cladding, a 220-nm Si guiding layer, and a 1 μm air upper cladding. Although a bottom cladding thickness of 2–3 μm is typically used in PICs, the light propagating in the waveguide barely interacts with the underlying Si substrate. Therefore, a 1 μm oxide cladding terminated with a perfectly matched layer (PML) was adopted, effectively assuming a semi-infinite silicon oxide region below the waveguide.

We set the waveguide width to 1 μm so that the waveguide supports the fundamental TE-like mode and the first higher-order TE-like mode, denoted here as TE_{00} and TE_{10}, respectively (see Supporting Section S1 Fig. S1). Two input waveguides, each with a width of 1 μm, are positioned on the left side of the structure and separated by a 1 μm gap.

We model the input excitation as a Gaussian pulse centered at $\lambda_0 = 1.55\,\mu$m with a frequency bandwidth of $\Delta f = 0.1c/a$, where $a = 1\,\mu$m. This bandwidth corresponds approximately to a wavelength range of 1.4–1.7 μm. Unless otherwise specified, we launch the pulses into the two input waveguides simultaneously and with the same initial phase. The input combinations of waveguide modes are (TE_{00}, TE_{00}), (TE_{00}, TE_{10}), (TE_{10}, TE_{00}), and (TE_{10}, TE_{10}), which correspond to the (0,0), (0,1), (1,0), and (1,1) input signals, respectively.

The optical fields then propagate through a $4 \times 4\,\mu\text{m}^2$ free-form design region and couple into a single output waveguide with a width of 1 μm. We include an additional 1 μm padding region along the in-plane (x and y) directions and terminate the three-dimensional simulation domain with 1 μ m-thick perfectly matched layers on all boundaries. We perform the optimization using an electromagnetic simulation resolution of 20 pixels/μm (Δx=Δy=Δz =50 nm). After optimization, we re-evaluate the final device at a higher simulation resolution of 50 pixels/μm (Δx=Δy=Δz =20 nm) to verify the device performance and reduce discretization-induced numerical error [43], [44].

$$\tau = \frac{P_{\text{out}}}{P_{\text{src}}}, \tag{1a}$$

$$P_\alpha = \frac{1}{2}\text{Re}\left[\int_A (\mathbf{E}_\alpha \times \mathbf{H}_\alpha^*)\cdot \hat{\mathbf{n}}\, dA\right], \qquad \alpha \in \{\text{out}, \text{src}, \text{tar}\}, \tag{1b}$$

$$\xi = \frac{\left|\int_A (\mathbf{E}_{\text{out}} \times \mathbf{H}_{\text{tar}}^*)\cdot \hat{\mathbf{n}}\, dA\right|^2}{4P_{\text{out}}P_{\text{tar}}}, \tag{1c}$$

$$\mathcal{T} = \tau\xi. \tag{1d}$$

To quantify device performance, we define a normalized figure of merit (FoM) that measures the target-mode power normalized to the single-port input power. The FoM combines two quantities: the normalized transmitted power τ and the modal purity ξ, as summarized in (1).

The normalized transmitted power τ, defined in (1a), is the ratio of the total output power P_{out} to the input power P_{src} injected into a single input waveguide. We normalize τ to the power launched from a single input waveguide to provide a per-port power reference that can be compared consistently across logical input states and potential downstream connections. Since the two-input configuration simultaneously excites two input waveguides with equal single-port input powers, the total incident power corresponds to 2 under this normalization. This convention does not imply that arbitrary coherent cascading of independently optimized gates is established by the present work. In a cascaded configuration, the output of one gate is recoupled into a single input port of the next gate, so its power level must be directly comparable to the single-port input power P_{src}. The input power P_{src} is set to be the same for both TE_{00} and TE_{10} excitations ($P_{\text{src,TE}_{00}} \approx P_{\text{src,TE}_{10}}$), ensuring that τ is independent of the input mode combinations and can be directly compared across different logic states. Consequently, τ takes values in the range $\tau \in [0, 2]$.

Each power P_α is computed from the time-averaged Poynting flux through the corresponding waveguide cross-section, as given in (1b), where $\hat{\mathbf{n}}$ denotes the propagation direction normal to the cross-section and A is the cross-sectional area. Here, $\mathbf{E}_{\text{out}}$ and $\mathbf{H}_{\text{out}}$ denote the fields obtained at the output port from the full 3D FDTD simulation, $\mathbf{E}_{\text{src}}$ and $\mathbf{H}_{\text{src}}$ denote the fields launched into a single input waveguide, and $\mathbf{E}_{\text{tar}}$ and $\mathbf{H}_{\text{tar}}$ denote the reference eigenmode fields of the target output mode.

We then evaluate the modal purity by calculating the normalized overlap between the simulated output field and the target mode field, as defined in (1c). The modal purity satisfies $\xi \in [0, 1]$, approaching unity when the field reaching the output waveguide matches the desired target mode and decreasing when the output-waveguide power is distributed among undesired guided modes [45]. Radiation loss primarily reduces the normalized transmitted power τ, while the combined quantity $T = \tau\xi$ accounts for both power delivery to the output waveguide and modal selectivity.

Finally, the overall FoM is defined as the product of these two quantities, as given in (1d). This combined metric captures both the device's transmission efficiency and modal selectivity. Throughout this work, we encode the logical states "0" and "1" using the TE_{00} and TE_{10} spatial modes, respectively. For each input combination, we evaluate two FoMs at the output port: one for the target mode specified by the logic truth table and the other for the undesired opposing mode. The target-mode FoM quantifies the transmission efficiency into the correct logical output, whereas the opposing-mode FoM quantifies modal crosstalk. For example, in the AND gate, the input combination (TE_{10}, TE_{10}) corresponds to the logical input (1,1) and therefore requires a TE_{10} output. In this case, the FoM evaluated with respect to TE_{10} corresponds to the desired transmission, while the FoM evaluated with respect to TE_{00} corresponds to crosstalk. For the other AND-gate input combinations, the truth table requires a logical "0" output, so TE_{00} and TE_{10} exchange these roles. For each input combination, we denote the FoMs evaluated for the truth-table-prescribed target mode and the opposing logical mode as $T_{m,\text{tar}}$ and $T_{m,\text{opp}}$, respectively. In the optimization notation below, trs labels the target-mode transmission objective, whereas ct labels the opposing-mode crosstalk objective.

$$\min_{\boldsymbol{\rho}, t} \quad t \tag{2a}$$

$$\text{s.t.} \quad \nabla \times \frac{1}{\mu_0\mu_r}\nabla \times \mathbf{E}_m - \omega_0^2\epsilon_0\boldsymbol{\epsilon}_r(\boldsymbol{\rho})\mathbf{E}_m = -i\omega_0\mathbf{J}_m, \quad m \in \{00,\ 10,\ 01,\ 11\}, \tag{2b}$$

$$\lambda_0 = 1550\,\text{nm}, \qquad \omega_0 = 2\pi c/\lambda_0,$$

$$0 \le \boldsymbol{\rho} \le 1, \tag{2c}$$

$$f_{m,l}(\boldsymbol{\rho}) - t \le 0, \quad \begin{cases} f_{m,\text{trs}} = 1 - \mathcal{T}_{m,\text{tar}}, \\ f_{m,\text{ct}} = \mathcal{T}_{m,\text{opp}}, \end{cases} \quad m \in \{00,\ 10,\ 01,\ 11\}, \qquad l \in \{\text{trs},\ \text{ct}\}, \tag{2d}$$

$$g_k(\boldsymbol{\rho}) \le 0, \quad k \in \{\mathrm{LW}, \mathrm{LS}\}. \tag{2e}$$

We adopt the minimax formulation described in (2) to balance multiple competing objectives across all input combinations and output channels [46]. The auxiliary variable t in (2a) converts the multi-objective optimization into an epigraph minimax form, so the optimizer minimizes the worst-case objective among all truth-table conditions. This formulation minimizes the worst-case objective value, thereby preventing the optimizer from improving one logic condition at the expense of others. We solve the resulting constrained optimization problem using the Method of Moving Asymptotes (MMA) [47], implemented through the open-source `NLopt` library [48]. MMA efficiently handles nonlinear inequality constraints and gradient-based design updates, making it well-suited for adjoint-based topology optimization.

Equation (2b) defines the electromagnetic constraint for the optimization problem. It represents the time-harmonic Maxwell wave equation for the electric field $\mathbf{E}_m$ generated by the source current density $\mathbf{J}_m$ at angular frequency ω_0. The relative permittivity distribution $\boldsymbol{\epsilon}_r(\boldsymbol{\rho})$ depends on the design variable $\boldsymbol{\rho}$ and determines the optical response of the free-form design region. In this work, we optimize the device at a single wavelength of $\lambda_0 = 1.55\,\mu$m, corresponding to $\omega_0 = 2\pi c/\lambda_0$, and evaluate the broadband response separately after optimization in Section III. By including Maxwell's equation as a constraint, the optimization ensures that every objective function $f_{m,l}$ is evaluated using electromagnetic fields that are physically consistent with the current design $\boldsymbol{\rho}$ at each iteration.

In (2c), $\boldsymbol{\rho}$ represents the density variable defined at each pixel of the design region. We map $\boldsymbol{\rho}$ continuously to the relative permittivity of the structure, where $\boldsymbol{\rho} = 0$ corresponds to air ($\varepsilon_r = 1.00$) and $\boldsymbol{\rho} = 1$ corresponds to silicon ($\varepsilon_r = 12.08$). We initialize the fixed input- and output-waveguide regions as either air or silicon according to the prescribed layout, while assigning the remaining free-form design region a uniform intermediate density of $\rho = 0.5$. This initialization provides an unbiased starting point for topology optimization.

In (2d), we define the transmission objective as a loss, $f_{m,\mathrm{trs}} = 1 - \mathcal{T}_{m,\mathrm{tar}}$, where $\mathcal{T}_{m,\mathrm{tar}}$ denotes the FoM evaluated for the truth-table-prescribed target mode. We define the crosstalk objective as $f_{m,\mathrm{ct}} = \mathcal{T}_{m,\mathrm{opp}}$, where $\mathcal{T}_{m,\mathrm{opp}}$ denotes the FoM evaluated for the undesired opposing mode. This formulation simultaneously maximizes transmission into the desired output mode and suppresses coupling into the undesired mode across all four input combinations. The geometric constraints g_{LW} and g_{LS} impose the minimum line width and line spacing requirements, respectively, to promote fabrication-compatible designs. Finally, the constraints $g_k \le 0$ in (2e) enforce the minimum line-width (LW) and line-spacing (LS) requirements, as described in (4)

$$\widetilde{\boldsymbol{\rho}}(\mathbf{x}) = \int_{\Omega_\mathrm{D}} w(\mathbf{x} - \mathbf{x}')\, \boldsymbol{\rho}(\mathbf{x}')\, d\mathbf{x}', \tag{3a}$$

$$w(\mathbf{r}) = \begin{cases} \frac{1}{C(\mathbf{x})}\left(1 - \frac{|\mathbf{r}|}{R}\right), & |\mathbf{r}| \le R, \\ 0, & |\mathbf{r}| > R, \end{cases} \tag{3b}$$

$$\bar{\boldsymbol{\rho}}(\mathbf{x}) = \frac{\tanh(\beta\eta) + \tanh[\beta\,(\widetilde{\boldsymbol{\rho}}(\mathbf{x}) - \eta)]}{\tanh(\beta\eta) + \tanh[\beta(1-\eta)]}. \tag{3c}$$

We apply a conic density filter followed by a hyperbolic-tangent threshold projection to promote a smooth and nearly binary material distribution [46], [49]. In (3a), $\boldsymbol{\rho}$ denotes the raw design density, $\widetilde{\boldsymbol{\rho}}$ denotes the filtered density, and Ω_D denotes the design domain. The conic kernel $w(\mathbf{r})$ averages the density over a circular neighborhood with radius R, where $\mathbf{r} = \mathbf{x} - \mathbf{x}'$, as described in (3b). The normalization factor $C(\mathbf{x})$ ensures that the filter weights integrate to unity at each position, including points near the boundary of the design domain. This filtering step suppresses checkerboard patterns and sub-resolution features that can arise during topology optimization.

The projection function in (3c) maps the filtered density $\widetilde{\boldsymbol{\rho}}$ to the projected density $\bar{\boldsymbol{\rho}}$. The parameter $\eta \in [0, 1]$ sets the projection threshold, while β controls the steepness of the transition between the low- and high-index materials. Increasing β gradually sharpens the material interface and drives the optimized structure toward a binary distribution. Together with the minimum line-width and line-spacing constraints introduced above, this filtering and projection procedure improves fabrication compatibility while retaining differentiability for adjoint-based gradient optimization.

In this work, we choose the filter radius R such that the optimization suppresses features smaller than approximately 50 nm during binarization. We evaluate this minimum-feature-size condition using an eroded projection threshold of $\eta_e = 0.75$. We perform the optimization over 15 epochs, with 100 iterations per epoch. The projection parameter β starts from $\beta = 2$ and doubles after each epoch until it reaches $\beta = 2^{15}$. This continuation strategy gradually sharpens the material distribution while allowing the topology to evolve during the early stages of optimization.

$$g_{LW} = \frac{1}{n}\sum_{i\in\mathbb{N}} I_i^{LW}(\boldsymbol{\rho}) \cdot \left[\min\{\widetilde{\rho}_i - \eta_e,\, 0\}\right]^2, \tag{4a}$$

$$I_i^{LW}(\boldsymbol{\rho}) = \bar{\boldsymbol{\rho}}_i \cdot \exp\!\left(-c\,|\nabla\widetilde{\boldsymbol{\rho}}_i|^2\right), \tag{4b}$$

$$g_{LS} = \frac{1}{n}\sum_{i\in\mathbb{N}} I_i^{LS}(\boldsymbol{\rho}) \cdot \left[\min\{\eta_d - \widetilde{\rho}_i,\, 0\}\right]^2, \tag{4c}$$

$$I_i^{LS}(\boldsymbol{\rho}) = (1 - \bar{\boldsymbol{\rho}}_i) \cdot \exp\!\left(-c\,|\nabla\widetilde{\boldsymbol{\rho}}_i|^2\right). \tag{4d}$$

Although the conic filter and threshold projection promote smooth and nearly binary structures, they do not by themselves impose an explicit lower bound on the feature dimensions. The conic filter suppresses sub-resolution features through spatial averaging, while the threshold projection sharpens the filtered density profile. However, small, isolated silicon or air features can remain after projection if no additional geometric constraints are applied.

To further improve fabrication compatibility, we impose the minimum-linewidth and minimum-linespacing constraints defined in (4a)–(4d) [46], [50]. Here, g_{LW} penalizes silicon features that violate the prescribed minimum linewidth, whereas g_{LS} penalizes air gaps that violate the prescribed minimum

spacing. The index set $\mathbb{N}$ contains the design pixels, and n denotes the total number of pixels used in the constraint evaluation. The indicator functions I_i^{LW} and I_i^{LS} localize the penalties to solid-like and void-like regions, respectively. At the same time, the exponential term reduces the contribution from material interfaces where the density gradient is large. By enforcing $g_{LW} \leq 0$ and $g_{LS} \leq 0$, the optimizer suppresses linewidth and spacing violations within the prescribed numerical tolerance.

Here, η_e and η_d denote the eroded and dilated projection thresholds, respectively, and define the density levels used to identify linewidth and linespacing violations. The squared minimum terms, $[\min\{\cdot, 0\}]^2$, quantify the magnitude of each constraint violation. The exponential factor, which contains the convergence coefficient c, reduces the contribution from pixels with large density gradients, thereby suppressing interface-dominated contributions and focusing the penalty on feature interiors. Specifically, g_{LW} penalizes solid-like regions whose filtered density falls below the eroded threshold η_e, whereas g_{LS} penalizes void-like regions whose filtered density exceeds the dilated threshold η_d. These two constraints therefore suppress silicon features and air gaps that are smaller than the prescribed minimum feature size.

In this work, we first optimize the structure for 15 epochs without geometric constraints, allowing the topology to explore a broad design space. We then activate the minimum-linewidth and minimum-linespacing constraints in the final, 16th epoch to refine the design toward a fabrication-compatible binary structure. This staged optimization strategy improves the manufacturability of the final device while preserving the optical performance obtained during the unconstrained optimization stage.

B. Device Fabrication

We fabricate the devices on a 220-nm-thick SOI wafer, which we dice into $8 \times 8\,\text{mm}^2$ chips. We sequentially clean the chips using N-methyl-2-pyrrolidone, acetone, and isopropyl alcohol (IPA) to remove organic residues and surface contaminants. We then spin-coat ZEP 520A electron-beam resist at 4000 rpm for 40 s and bake the coated chips on a hotplate at $180\,^\circ\text{C}$ for 5 min.

We define the patterns of each logic gate using electron-beam lithography. After exposure, we develop the resist in ZED-N50 for 2 min 30 s, rinse it in methyl isobutyl ketone for 30 s, and finally rinse it in IPA. We transfer the exposed patterns into the silicon device layer using inductively coupled plasma reactive-ion etching with fluorocarbon-based chemistry. Finally, we characterize the fabricated devices using scanning electron microscopy.

III. Results and Discussion

Unless otherwise stated, all field distributions, transmission characteristics, modal crosstalk, and SNR values presented in this section are obtained from electromagnetic simulations.

A. Device Performance

This section evaluates the inverse-designed photonic logic gates described in the previous section. We design six two-input, single-output logic gates, including AND, OR, XOR, NAND, NOR, and NXOR, within the same $4 \times 4\,\mu\text{m}^2$ design region on a SOI platform. All devices are optimized at the target wavelength of $\lambda_0 = 1.55\,\mu\text{m}$. For each gate, the optimization maximized coupling into the truth-table-prescribed output mode while suppressing coupling into the opposing mode. This design strategy allows us to evaluate whether the proposed mode-encoded architecture can realize reference-light-free operation, broadband response, and phase-controlled reconfigurability within a compact footprint.

Fig. 3 shows the optimization history of the XOR gate as a function of iteration number. During the first epoch, which corresponds to the initial 100 iterations, the optimizer rapidly establishes the main topology of the free-form design region. In subsequent epochs, we gradually increase the projection sharpness parameter β, which drives the density distribution toward a more binary and fabrication-compatible structure, as shown in Fig. 3(c)–(e). The oscillatory behavior observed around iterations 100–200 and 700–800 reflects the difficulty of balancing multiple competing objectives, including high transmission into the target mode and low crosstalk into the opposing mode for all input combinations. These oscillations suggest that the optimizer temporarily explores regions near local optima or flat regions of the objective landscape. However, doubling of the projection parameter β modifies the optimization landscape, allowing the design to further evolve toward an improved topology. As a result, the target-mode FoM remains high while the crosstalk FoM decreases, indicating that the optimization successfully converges to a mode-selective XOR logic device.

When we activate the geometric constraints in the final epoch, the optimizer removes features that violate the prescribed fabrication rules. This constraint activation can cause an abrupt degradation in optical performance, as reported in previous fabrication-constrained inverse-design studies [46]. We observe the same behavior in our optimization.

To reduce this performance drop, we sweep the convergence coefficient $c \in \{10^{-5}, 10^{-6}, 10^{-7}, 10^{-8}\}$ and the minimum feature length $L_{\min} \in \{0.02, 0.03, 0.04, 0.05\}\,\mu\text{m}$. We then select the final constrained design using the following procedure:

1) We exclude the $L_{\min} = 0.02\,\mu\text{m}$ cases because this feature size lies below the target fabrication limit.
2) Among the remaining candidates, we identify the five designs with the highest worst-case SNR in the four input combinations.
3) From these five candidates, we retain the three designs with the highest total SNR.
4) Among the remaining three candidates, we select the design with the lowest standard deviation of the SNR across the four input combinations.

This selection procedure favors designs that produce a reliable output signal for every truth-table input condition

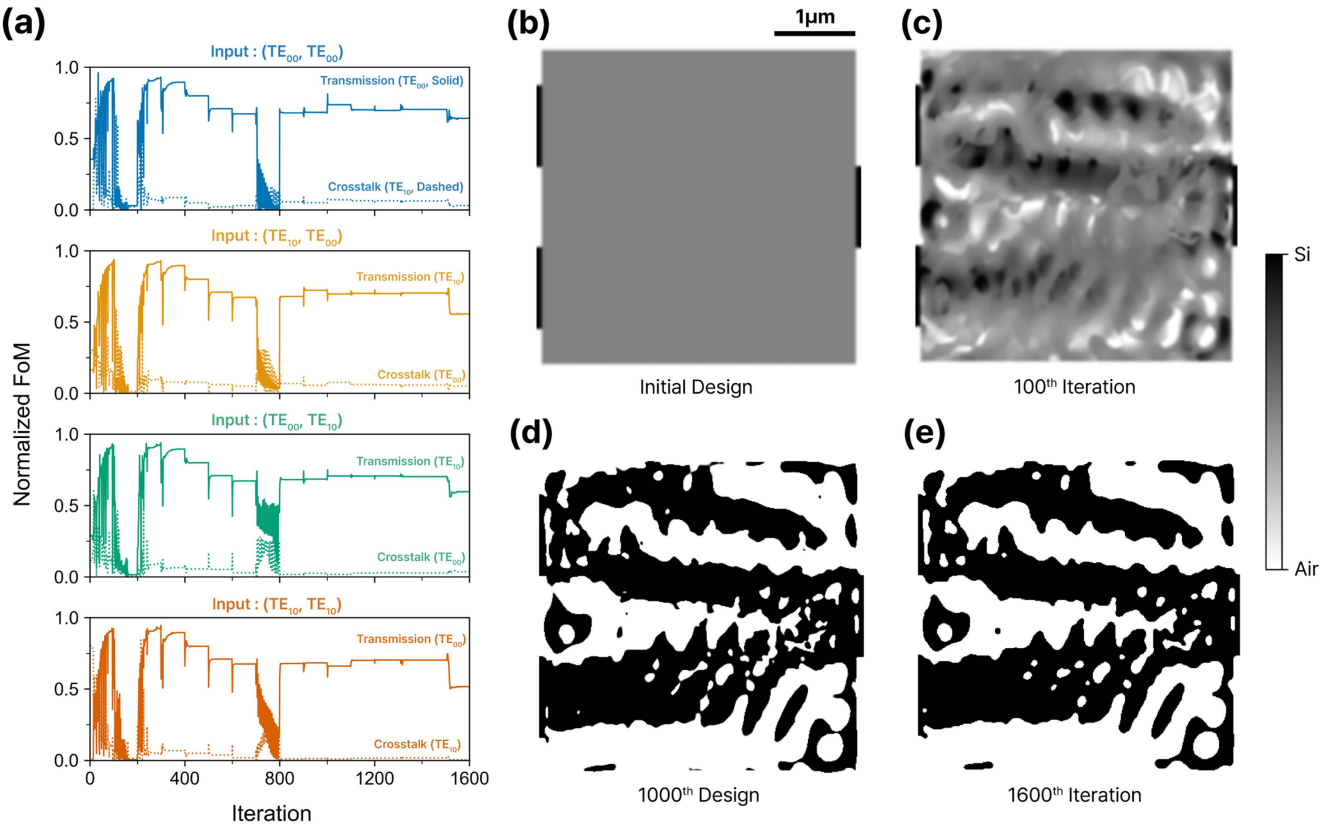

Fig. 3. Optimization process of the inverse-designed mode-encoded logic gate. (a) Evolution of the normalized figure of merit (FoM) during optimization for the four input-mode combinations: (TE_{00}, TE_{00}), (TE_{10}, TE_{00}), (TE_{00}, TE_{10}), and (TE_{10}, TE_{10}). Solid curves indicate the FoM for transmission into the truth-table-prescribed target mode, while dashed curves indicate crosstalk into the opposing mode. The optimization increases the target-mode transmission while suppressing modal crosstalk for all input combinations. (b)–(e) Evolution of the material distribution in the $4 \times 4\,\mu\mathrm{m}^2$ design region: (b) initial uniform density distribution, (c) intermediate continuous-density structure after 100 iterations, (d) near-binary structure after 1000 iterations, and (e) final optimized structure after 1600 iterations. Black and white regions correspond to silicon and air, respectively.

TABLE I
SIMULATED AVERAGE TRANSMISSION AND SNR OF THE SIX OPTIMIZED LOGIC GATES EVALUATED AT $\lambda_0 = 1.55\,\mu\mathrm{m}$. TRANSMISSION IS REPORTED AS A LINEAR RATIO BETWEEN 0 AND 2; SNR IS DEFINED AS $10\log_{10}(T/CT)$.

Gate	Average transmission	Average SNR (dB)
AND	0.439	10.1
OR	0.516	7.9
XOR	0.532	15.0
NAND	0.420	6.7
NOR	0.306	8.3
NXOR	0.371	9.5

while maintaining high overall SNR and balanced performance across different inputs. For the XOR gate, this procedure selects the design obtained with $L_{\min} = 0.04\,\mu\mathrm{m}$ and $c = 10^{-8}$. Supporting Section S3 provides the detailed sweep results.

Fig. 4 and Table I verify the reference-light-free truth-table operation of the proposed mode-encoded logic gates, re-evaluated using the 50 pixels/μm verification simulations. We optimized six two-input logic functions, AND, OR, XOR, NAND, NOR, and NXOR, and evaluated each device for the four possible input combinations. For each case, the solid bar represents the FoM associated with the truth-table-prescribed output mode, while the hatched bar represents the FoM associated with the undesired opposing mode. The target-mode FoM consistently exceeds the crosstalk FoM for every gate and input state, demonstrating that the inverse-designed region performs the intended mode conversion according to the desired logic function.

Fig. 4(a) shows the truth-table responses of the six optimized logic gates at 1550 nm, where the target-mode transmission is compared with the corresponding logical crosstalk for each input combination. Although the transmission efficiency varies across the gates and input states because each device must satisfy multiple competing mode-conversion conditions within the same compact footprint, all optimized devices maintain a clear separation between the desired and undesired output modes. This modal selectivity confirms that binary logic can be implemented using spatial-mode encoding, even for gates such as NAND and NOR that are difficult to realize in passive intensity-encoded architectures without an additional bias or reference signal.

To further examine the origin of this modal selectivity, Fig. 4(b) separately presents the modal purity of the target and opposing logical modes. Because the SNR is determined by the relative power coupled to these two logical modes, the modal-purity distributions directly reveal the mode-selective behavior of each device. Despite variations among the gates and input combinations, the target-mode purity remains consistently higher than the purity of the opposing logical mode,

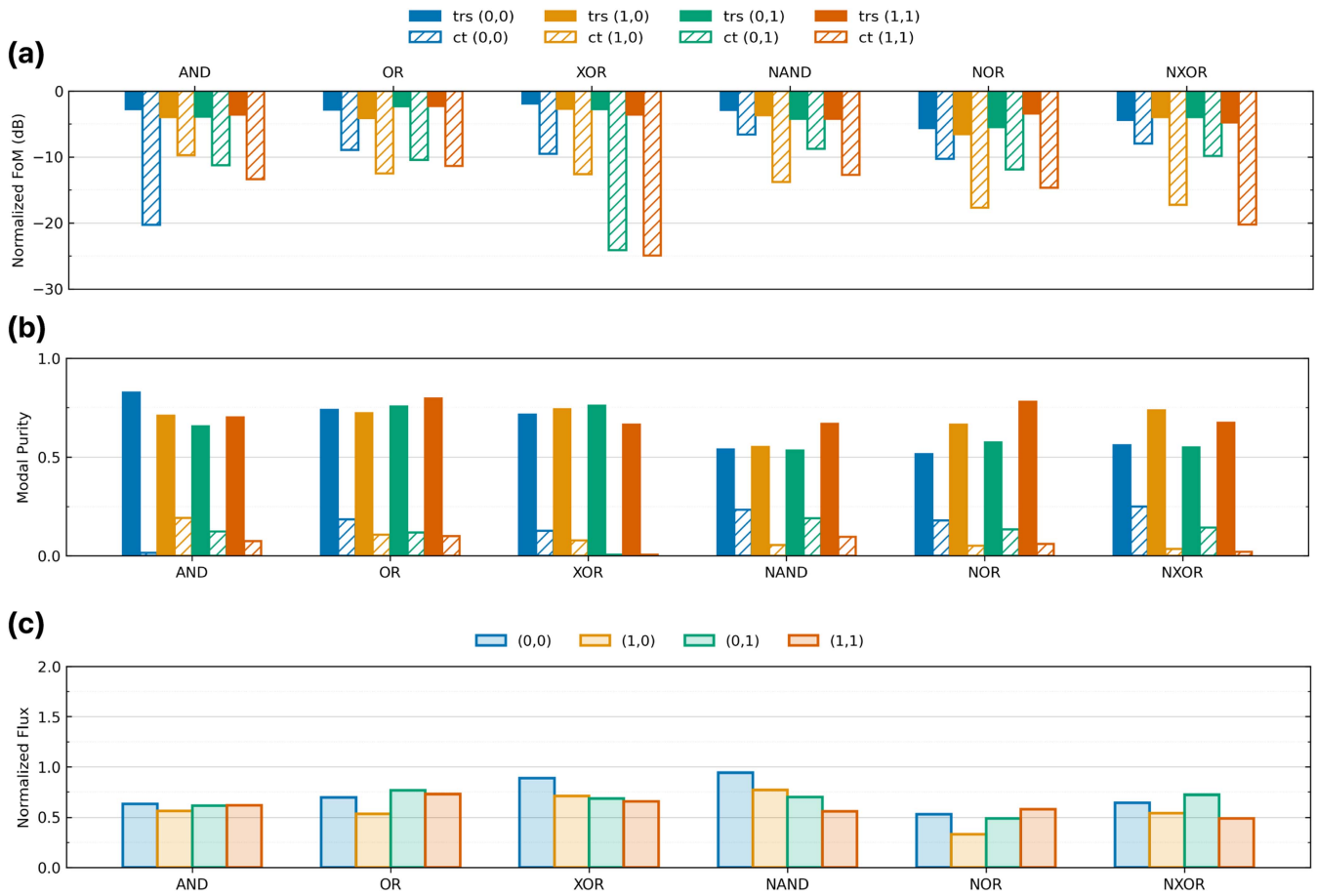

Fig. 4. Simulated truth-table performance of the inverse-designed mode-encoded photonic logic gates. (a) Normalized figures of merit (FoMs) for the six optimized logic gates, AND, OR, XOR, NAND, NOR, and NXOR, evaluated for all four input combinations, (0,0), (1,0), (0,1), and (1,1), where the logical states "0" and "1" are encoded by the TE_{00} and TE_{10} modes, respectively. Solid bars labeled "trs" indicate transmission into the truth-table-prescribed target output mode, whereas hatched bars labeled "ct" indicate crosstalk into the opposing logical mode. The FoMs are shown in decibels to highlight crosstalk suppression. (b) Modal purity of the target and opposing logical modes for the corresponding gates and input combinations. (c) Normalized total output flux for each gate and input combination. The output flux is normalized to the power launched from a single input waveguide; therefore, the total input power for the two-input configuration is normalized to 2.

confirming that the required modal separation is maintained for all truth-table states.

Fig. 4(c) further shows the normalized total output flux for each gate and input combination. Since the transmission FoM is determined by the product of the output flux and the corresponding modal purity, optimization must simultaneously promote power delivery to the output waveguide and selective coupling to the desired logical mode. The resulting devices retain substantial output flux while maintaining the modal separation shown in Fig. 4(b), indicating that the optimized truth-table responses are achieved through the combined control of output power and modal selectivity rather than through modal selectivity alone.

Across all gates and input combinations, the SNR remain above 3.53 dB and the transmission above 0.220, confirming that every optimized structure satisfies the truth-table response of its respective logic function. Among our optimized logic gates, the XOR gate exhibits the highest average SNR of 15.0 dB while maintaining an average transmission of 0.532. It is therefore selected as the representative device for the detailed analysis presented in the following sections.

Fig. 5 further analyzes the XOR gate as a representative example. Fig. 5(a) shows the scanning electron microscopy image of the fabricated device. The fabricated pattern closely follows the optimized free-form topology and preserves the minimum feature size constraints imposed during optimization. Fig. 5(b) presents the simulated optical intensity distributions for the four input combinations. In all cases, the output field forms the mode specified by the XOR truth table: the (0,0) and (1,1) inputs produce the logical "0" output, whereas the (1,0) and (0,1) inputs produce the logical "1" output. Fig. 5(c) shows the wavelength-dependent normalized FoM decomposed into several guided output modes, including TE_{00}, TE_{10}, TM_{00}, TE_{20}, and TM_{10}. The spectral response confirms that the device maintains XOR logic over a broad wavelength range centered on the design wavelength. The desired TE_{00} or TE_{10} output mode dominates for each input condition, while coupling to TM_{00} and TM_{10} remains negligible.

However, Fig. 5(b) also shows weak interference fringes in the output waveguide. The modal decomposition in Fig. 5(c) indicates that these fringes mainly originate from residual excitation

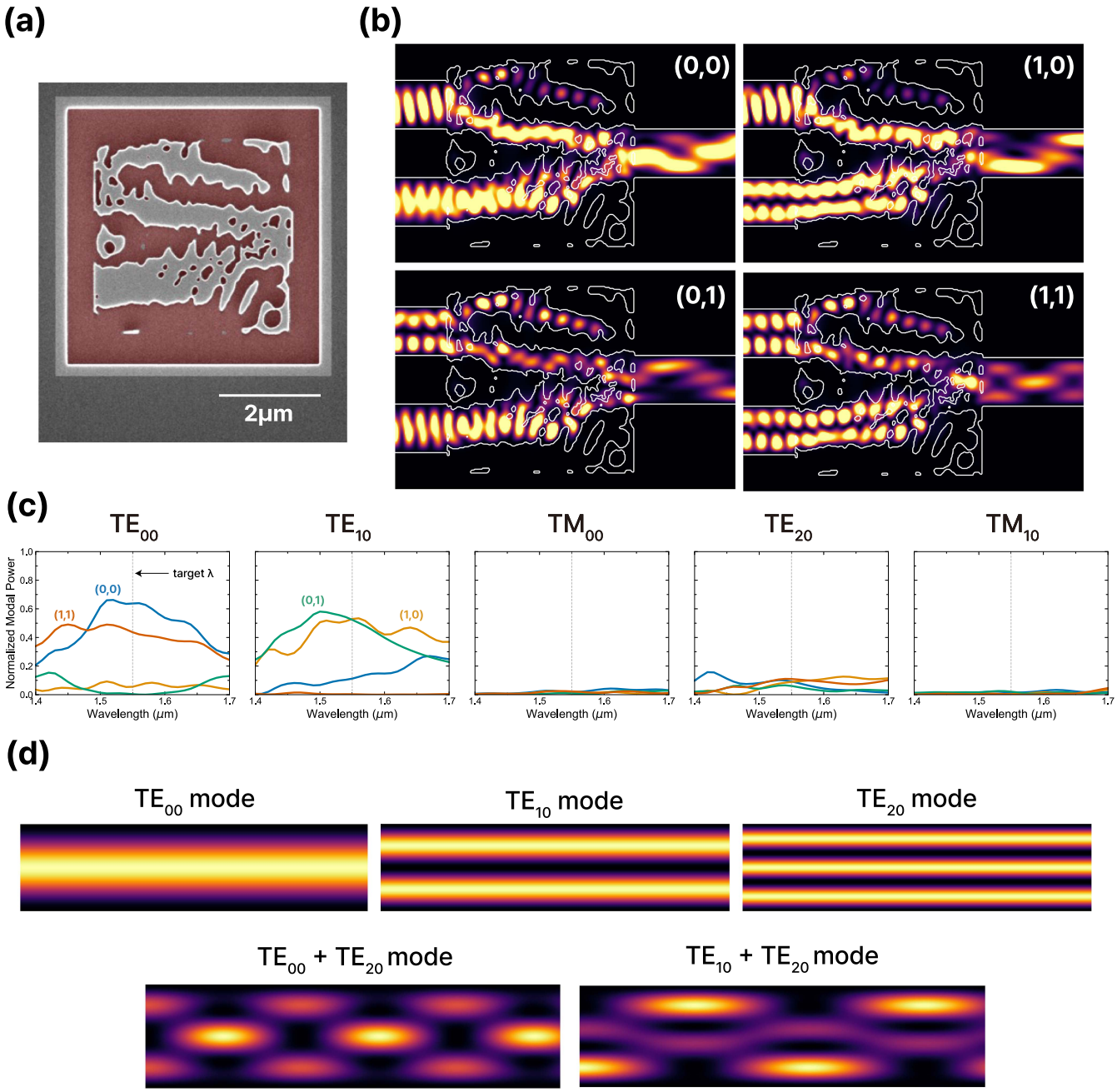

Fig. 5. Fabricated XOR gate and simulated modal analysis of its broadband response. (a) Scanning electron microscopy image of the fabricated inverse-designed XOR logic gate on the SOI platform. (b) Simulated electric-field intensity distributions for the four input combinations, (0,0), (1,0), (0,1), and (1,1), where the logical states "0" and "1" are encoded by the TE_{00} and TE_{10} input modes, respectively. The optimized free-form region converts the input-mode combination into the truth-table-prescribed output mode. (c) Spectral response of the XOR gate from 1.4 to 1.7 μm, evaluated by the normalized FoM for several output modes, including TE_{00}, TE_{10}, TM_{00}, TE_{20}, and TM_{10}. The vertical dashed line indicates the design wavelength of 1.55 μm. The device preferentially couples the (0,0) and (1,1) inputs to the TE_{00} output mode and the (1,0) and (0,1) inputs to the TE_{10} output mode, while maintaining low coupling to undesired TM_{00}, TM_{10}, and TE_{20} modes. (d) Representative transverse field profiles of the supported output modes and selected mode superpositions, used to interpret the modal content of the output field.

of the TE_{20} mode, which is not included as an optimization target. Because TE_{20} co-propagates with the desired output mode, its coherent superposition with TE_{00} or TE_{10} produces a spatial beating pattern in the output waveguide. Fig. 5(d) supports this interpretation by comparing the transverse field profiles of the individual modes and their coherent superpositions. The calculated superposition patterns reproduce the fringe features observed in the output field distributions. This higher-order-mode contamination can be reduced in future designs by adding a mode-demultiplexing unit at the output to filter unwanted modes. Alternatively, the device can be re-optimized using a narrower output waveguide, such as a 0.8 μm-wide waveguide, to reduce

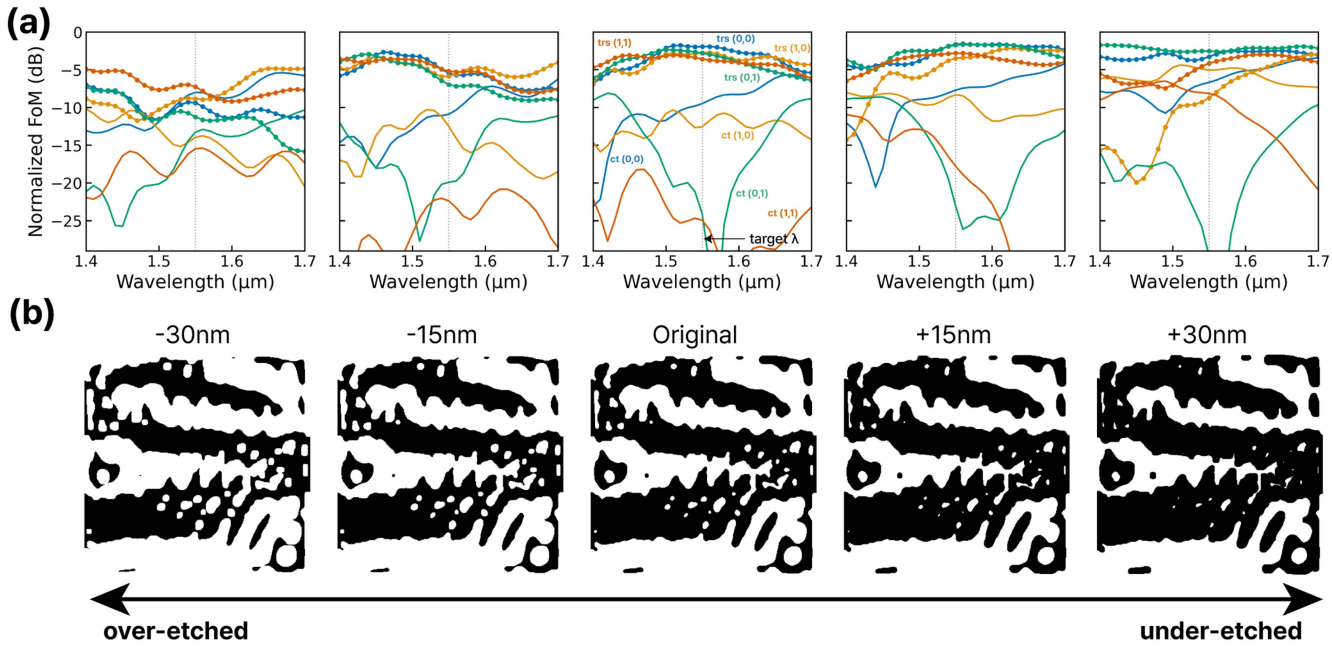

Fig. 6. Numerical tolerance analysis of the inverse-designed XOR gate under modeled etch-bias variations. (a) Wavelength-dependent normalized FoM of the XOR gate for five numerically generated geometry variations, -30 nm, -15 nm, original, $+15$ nm, and $+30$ nm etch bias. The negative and positive offsets represent over-etched and under-etched geometries, respectively. (b) Corresponding binary device geometries obtained by applying the etch-bias offsets to the optimized structure in simulation. These results are entirely numerical and do not represent experimental optical measurements of fabricated devices. The analysis evaluates how systematic fabrication deviations may affect the truth-table operation and the modal selectivity of the mode-encoded XOR gate.

the number of supported higher-order modes while preserving the TE_{00} and TE_{10} channels required for mode-encoded logic.

Next, we analyze the broadband response and fabrication tolerance of the XOR gate, which we optimize at the single wavelength of $\lambda_0 = 1.55\,\mu$m. Fig. 6(a), center, shows the spectral response of the original optimized structure over the 1.4–1.7 μm wavelength range. The device maintains an SNR greater than 5 dB across the 1.5–1.6 μm band, confirming that the XOR truth-table operation persists over a broad spectral window despite single-wavelength optimization. This is consistent with distributed multimode interference rather than a narrowband high-Q resonant response. In contrast to micro-ring-resonator-based devices, which rely on narrowband resonance, the proposed structure performs mode conversion through distributed interference among multiple guided modes. Although the inverse-designed geometry may contain localized features that introduce weak resonant perturbations, the spectra in Fig. 6(a) do not exhibit sharp high-Q resonant dips or peaks. The smooth spectral variation, therefore, indicates that narrowband resonances do not dominate the device response. Instead, distributed multimode interference governs the logic operation, enabling broadband performance around the design wavelength.

The fabrication sensitivity of the XOR gate was evaluated numerically by applying systematic etch-bias offsets to the optimized geometry, as shown in Fig. 6. The structure was computationally eroded or dilated by ± 15 nm and ± 30 nm, and the optical response of each modified geometry was recalculated using electromagnetic simulation. These results represent modeled fabrication deviations and do not correspond to experimental optical measurements of devices fabricated at different etch biases. These variations indicate that small fabrication errors perturb the accumulated modal phases and coupling strengths, but do not destroy the intended mode-conversion pathways. In contrast, geometry deviations of ± 30 nm lead to a noticeable degradation of the logic response. In these cases, the separation between the target-mode transmission and the opposing-mode crosstalk decreases, indicating that larger etch errors significantly disturb the optimized interference condition. These numerical results suggest that fabrication deviations should be maintained within approximately ± 15 nm for the modeled device to preserve the XOR response. The corresponding broadband and etch-tolerance analyses for the remaining logic gates are provided in Supporting Section S5, Figs. S19–S23.

We next investigate the wavelength-dependent response of the XOR gate as a function of the relative phase difference between the two input waveguides. The free-form multi-mode interference region operates as a coherent interference region, where the relative phase between the two inputs controls the interference condition and, consequently, the output modal distribution. Therefore, applying a phase shift to one input waveguide can modify the balance between constructive and destructive interference inside the design region while preserving the input modal basis of TE_{00} and TE_{10}. When the relative phase changes from 0 to π, the interference condition is inverted, thereby interchanging the dominant output power between the TE_{00} and TE_{10} modes and switching the corresponding logic response.

In the simulation, the prescribed relative phase is imposed directly through the complex source amplitude. Specifically, a phase factor of $\exp(i\Delta\phi)$ is applied to one input excitation while the other input is used as the phase reference. Propagation from the source planes to the inverse-designed region is included in the electromagnetic simulation, including the

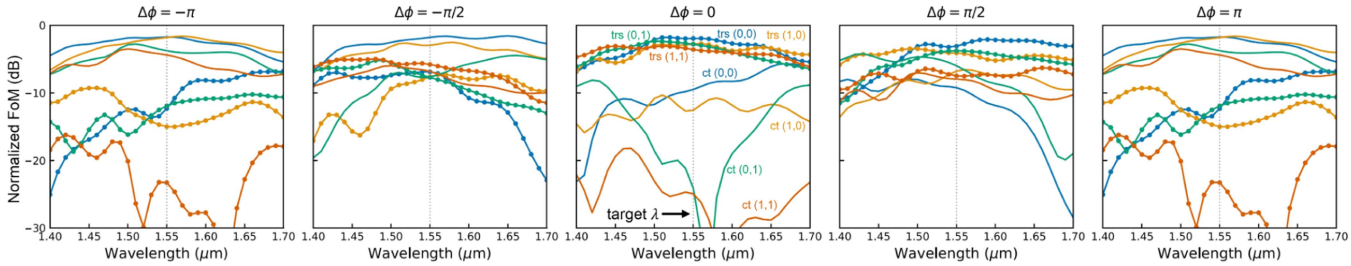

Fig. 7. Simulated phase-dependent spectral response of the inverse-designed mode-encoded logic gate. Wavelength-dependent normalized FoM of the optimized device for different relative phase differences between the two input waveguides, $\Delta\phi = -\pi$, $-\pi/2$, 0, $\pi/2$, π. For each phase condition, the spectra show the target-mode transmission (trs) and opposing-mode crosstalk (ct) for the four input combinations, (0,0), (1,0), (0,1), and (1,1). The vertical dashed line indicates the design wavelength of $\lambda_0 = 1.55\,\mu$m.

mode-dependent phase accumulation associated with the different propagation constants of TE_{00} and TE_{10}. As shown in Fig. 7, the XOR response obtained at $\Delta\phi = 0°$ is inverted at $\Delta\phi = \pm 180°$, resulting in the complementary NXOR operation.

In a practical silicon photonic circuit, the different effective indices of TE_{00} and TE_{10} must be considered when establishing this relative input phase. A suitable implementation is a mode-selective thermo-optic phase shifter based on a subwavelength-grating waveguide [51]. Such a device has been experimentally demonstrated for the first two TE modes in a 220-nm-thick silicon waveguide. When a mode-selective thermo-optic phase shifter is combined with a mode-insensitive thermo-optic phase shifter, the two modal phases can be controlled independently. This configuration could therefore compensate the different phase accumulation of TE_{00} and TE_{10} and provide the relative input phase required for phase-controlled XOR-to-NXOR switching.

B. Discussions

In this work, we use inverse-design-based topology optimization to design optical mode-encoded logic gates on a SOI platform. Although we optimize the devices at a single wavelength, the XOR gate maintains an SNR exceeding 5 dB across the 1.5–1.6 μm wavelength band. We also show that a single physical structure can implement both XOR and NXOR operations by controlling the relative phase between the two input signals. These results indicate that distributed interference among multiple guided modes is important for broadband and phase-reconfigurable logic operation.

However, several limitations remain. A first limitation of the present devices is their relatively limited target-mode transmission. In a passive cascaded configuration, the optical power delivered to successive stages is multiplied by the transmission efficiency of each preceding stage. Repeated stages with transmission below unity can therefore lead to rapid attenuation, limiting multistage operation. Fan-out imposes an additional power constraint because the available output power must be distributed among multiple downstream branches.

To identify the origin of the limited transmission, we decompose the optical power into the target logical mode, opposing logical mode, higher-order guided modes, reflection, and radiation contributions, as described in Supporting Section S6. At 1550 nm, the radiation contribution ranges from 0.77 to 1.40 under the single-input normalization and represents the largest non-target contribution for the investigated gates and input states. The reflected guided-mode power ranges from 0.15 to 0.52. Coupling to higher-order guided modes is smaller but can be comparable to or greater than the opposing logical-mode contribution for some input states.

These contributions affect cascading in different ways. Radiation removes power from the guided optical channels. Reflection reduces forward transmission and may introduce coherent feedback toward preceding stages. Higher-order-mode coupling retains power in the waveguide but transfers it outside the logical TE_{00} and TE_{10} basis. Improving the power efficiency of future devices may therefore require explicit suppression of radiation, reflection, and higher-order-mode excitation during optimization, together with additional design degrees of freedom where appropriate.

For cascading, the phase of the output field must also be considered. Because TE_{00} and TE_{10} have different propagation constants, they accumulate different phases while propagating through a multimode interconnect. For a fixed operating wavelength, a deterministic propagation-phase offset could be compensated by selecting an appropriate waveguide length. Active compensation could instead be implemented using combined mode-selective and mode-insensitive phase shifters, which provide independent control of the two modal phases [51]. The latter approach is more suitable when tunable phase correction is required.

The output-phase analysis in Supporting Section S7.2 shows, however, that the optimized devices generally produce input-state-dependent output phases, including among input states corresponding to the same logical output mode. Consequently, compensation of the propagation-induced phase difference between TE_{00} and TE_{10} cannot, by itself, guarantee the phase relations required for arbitrary coherent cascading of the present logic gates.

To determine whether this behavior originates from the particular inverse-designed geometries or from a more fundamental property of the architecture, we analyze the logic operations using linear scattering relations. The complex output amplitudes associated with the four Boolean input states are linked by linear

superposition and therefore cannot be specified independently. Consequently, the target- and opposing-mode responses and relative output phases cannot, in general, be independently prescribed. The resulting constraints depend on the specific Boolean operation. For example, the AND operation admits a nontrivial solution in which the target outputs are constrained to have identical phases, but this condition necessarily reduces the achievable worst-case SNR. In contrast, for the XOR operation, the linear scattering relations do not admit a corresponding nontrivial solution that simultaneously preserves the required truth-table response and imposes identical phases between states producing the same logical output. The corresponding conditions for the other Boolean operations are summarized in Supporting Section S8. Importantly, the equality solutions should be interpreted as bounds on the achievable worst-case SNR under the stated normalization and symmetry conditions, rather than as upper bounds on the SNR of every individual input state. The theoretical analysis therefore identifies an intrinsic trade-off between the achievable worst-case SNR and output-phase uniformity in the present linear mode-encoded architecture.

We further examine these theoretical predictions through phase-constrained inverse design (Supporting Section S9), in which the relative phases of states producing the same logical output were restricted to within $\pm 15^{\circ}$. For the AND gate, the target- and opposing-mode responses approach a stable solution, while the relative output phases enter the prescribed range at an early stage of optimization and remain within this range despite small perturbations. A feasible nontrivial phase-constrained AND solution can therefore be obtained, although its worst-case SNR is substantially reduced compared with that of the phase-unconstrained design. A markedly different behavior is observed for the XOR gate. Although the relative output phases rapidly satisfy the imposed constraints, the target- and opposing-mode responses continue to exhibit substantial fluctuations and do not converge to a stable solution with a high SNR, resulting in a pronounced degradation of performance. Thus, arbitrary coherent cascading of the present linear architecture remains intrinsically restricted, and phase-aware optimization alone cannot generally remove this limitation for all Boolean operations.

These results indicate that output phase should be considered together with the target-mode transmission, opposing-mode crosstalk, and resulting SNR when designing cascaded mode-encoded logic circuits. While the present analysis identifies constraints on simultaneously controlling the output response and phase of individual logic gates, it does not exclude alternative cascading strategies or circuit architectures. For example, future implementations may employ additional phase-management elements or jointly optimize multiple logic stages rather than independently optimizing and directly cascading individual gates.

IV. Conclusion

In this work, we numerically demonstrated inverse-designed, mode-encoded optical logic gates on a silicon-on-insulator platform. By encoding logical states in guided spatial modes rather than optical intensity, the proposed devices enable passive, reference-light-free Boolean operation at the individual-gate level within a compact $4 \times 4\,\mu\mathrm{m}^2$ footprint. Here, reference-light-free operation denotes the absence of an additional optical reference or bias beam for generating the Boolean output and does not imply phase-insensitive operation or arbitrary coherent cascadability. Using adjoint-based topology optimization, we designed six representative Boolean gates, including AND, OR, XOR, NAND, NOR, and NXOR. We numerically verified their truth-table operation through mode-selective transmission and crosstalk suppression.

The optimized XOR gate maintained an SNR above 5 dB across the 1.5–1.6 μm wavelength band despite being optimized only at a single wavelength. This broadband response arises from distributed multimode interference rather than narrowband resonance, distinguishing the proposed devices from conventional MZI- and micro-ring-resonator-based optical logic gates. Simulations further show phase-controlled reconfigurability, in which the same physical structure switches between XOR and NXOR operations by tuning only the relative phase between the input signals. This result highlights the coherent and reconfigurable nature of the mode-encoded logic platform.

We further investigated the phase dependence of the mode-encoded logic gates and its implications for cascading. Linear-scattering analysis show that the output intensities and phases of the four Boolean states cannot be independently specified. Phase-constrained inverse design confirmed the resulting trade-off between output-phase control and SNR, with a substantially stronger performance degradation for the XOR gate than for the AND gate. These results show that both modal intensity and output phase must be considered when extending mode-encoded logic toward cascaded photonic circuits.

These results indicate that output phase should be considered together with Boolean operation when extending mode-encoded logic beyond individual devices. Future work may therefore investigate phase management, optimization strategies that explicitly account for both modal intensity and phase, and circuit architectures in which multiple optical transformations are designed together rather than independently cascading individual gates. Overall, these results demonstrate compact and reconfigurable mode-encoded Boolean logic elements and identify the power and phase conditions that must be addressed to extend them to multistage photonic circuits.

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