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REVIEW

Device-to-System Perspectives on Scalable Ising Machines for Physics-Driven Computing

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ABSTRACT

Combinatorial optimization problems (COPs) are fundamental to numerous applications but remain challenging due to their exponentially large solution spaces and the limitations of conventional computing architectures. Ising machines have emerged as a promising alternative by mapping optimization problems onto the energy minimization of the Ising Hamiltonian. Various hardware implementations, including quantum annealers, digital annealers, and coherent Ising machines, have been explored based on distinct physical mechanisms. More recently, emerging device-based approaches have gained significant attention for their potential to enable scalable and energy-efficient optimization. In this review, we present a comprehensive overview of Ising machines from both theoretical and hardware perspectives, with particular emphasis on three emerging-device-based platforms: crossbar array-based, stochastic p-bit, and oscillator-based Ising machines. We establish a comparative device-to-system perspective that traces how distinct physical and device properties translate into computational primitives, hardware architectures, and ultimately system-level scalability. Platform-specific bottlenecks, including array nonidealities and peripheral overhead in crossbar-based systems, device variability and probability-generation overhead in p-bit systems, and synchronization and coupling-network complexity in oscillator-based systems, are quantitatively and qualitatively analyzed. Finally, we discuss future directions toward scalable and energy-efficient Ising hardware through device-to-system co-optimization across devices, circuits, architectures, and algorithms.

1 | Introduction

Combinatorial optimization problems (COPs) arise in a wide range of practical domains, including logistics planning, VLSI layout design, shortest path problems, and max-cut. These problems form the computational backbone of many real-world decision-making systems, yet remain inherently difficult to solve due to their exponentially large solution spaces. Representative examples include the traveling salesman problem, Boolean satisfiability (SAT), and graph partitioning tasks, which are broadly relevant to applications in manufacturing, finance, artificial intelligence, machine learning, bioinformatics, and materials science [1–5]. Developing efficient methods for solving NP-complete problems could have a transformative impact across numerous fields, as they represent some of the most computationally intractable problems encountered in practice [6–9]. NP-complete problems constitute an important class of computationally challenging problems and are therefore widely used as representative benchmarks for evaluating optimization algorithms and hardware.

Despite their importance, solving large-scale combinatorial optimization problems remains challenging because the solution space grows rapidly with problem size, making efficient exploration increasingly difficult. Heuristic, approximation, and problem-specific algorithms are widely employed to obtain high-quality solutions within practical time constraints and can be highly effective for particular problem classes and instances. However, their performance depends strongly on problem struc-

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ture and scale, and the computational cost of iterative search can still increase substantially for large problem instances. When implemented on conventional von Neumann architectures, repeated state updates and cost-function evaluations can further incur considerable data-movement and computational overhead, degrading throughput and energy efficiency as the problem scale increases [10–12]. To address these limitations, alternative computing paradigms using physical processes for optimization have been actively explored. Among these, the Ising machine has emerged as a powerful framework for formulating combinatorial optimization problems [13]. By mapping binary decision variables to spin states and encoding cost functions into pairwise interactions, a wide range of optimization problems can be expressed as Ising Hamiltonian minimization problems. Based on this formulation, various Ising machines have been developed to minimize energy by directly exploiting physical dynamics. Representative implementations include quantum annealers [14], digital annealers [7], and coherent Ising machines [15]. Each approach explores the energy landscape using distinct physical mechanisms, such as quantum tunneling, stochastic updates, and optical coherence. Despite their demonstrated capabilities, these platforms still face practical limitations associated with connectivity, system complexity, power consumption, and hardware integration. These limitations have motivated increasing interest in emerging-device-based Ising machines that exploit intrinsic material and device properties to pursue more compact and energy-efficient hardware implementations while addressing system-level scalability constraints.

Alternatively, in-memory computing-based Ising machines, which perform computation directly within memory arrays, have recently attracted significant attention. These systems are often referred to as memristor-based Hopfield neural networks (mem-HNNs) [16]. Hopfield neural networks (HNNs) have gained considerable interest because their fundamental components such as spins, interaction matrices, and energy functions (Hamiltonians) closely resemble those of the Ising model, enabling a one-to-one correspondence between the two systems. Therefore, by mapping the objective function of a combinatorial optimization problem onto an equivalent Ising Hamiltonian, HNNs can be utilized as Ising solvers to find the minimum-energy configuration corresponding to the optimal solution. HNNs operate by minimizing an energy function defined over binary neurons and an N×N symmetric weight matrix with zero diagonal elements. However, a well-known limitation of this approach is that the system can become trapped in local energy minima. To mitigate this issue, the simulated annealing (SA) algorithm is often employed, which increases the likelihood of reaching the global minimum by probabilistically accepting energetically unfavorable state transitions to escape local minima during node updates [17]. Consequently, there is growing research interest in implementing SA mechanisms directly at the hardware level. This direct correspondence enables efficient hardware realization of Ising solvers, particularly when combined with in-memory computing architectures.

Alternative strategies that exploit intrinsic physical dynamics for deterministic or quasi-deterministic optimization have also been actively explored. Oscillator-based Ising machines (OIMs) represent an alternative approach that leverages continuous-time dynamics for optimization. In OIMs, each oscillator functions as a spin, with its phase encoding binary states. Under subharmonic injection locking (SHIL), a network of coupled oscillators forms a continuous dynamical system that naturally evolves toward low-energy configurations through phase synchronization. Various implementations have been demonstrated using LC oscillators [18, 19] and CMOS ring oscillators [20, 21]. However, these approaches often suffer from large footprint and limited scalability, limiting their practical applicability. More compact implementations based on emerging device technologies, such as insulator-to-metal transition (IMT) materials [22] and bistable devices including biristors [23], have also been explored. Accordingly, these emerging devices are being actively investigated to enable more compact, scalable, and energy-efficient oscillator-based Ising machines.

In this paper, we review the origin and historical development of Ising machines from both theoretical and hardware perspectives. We begin by introducing the fundamental principles of the Ising model and its connection to combinatorial optimization, followed by a comprehensive overview of hardware implementations, including quantum annealers, digital annealers, coherent Ising machines, and emerging-device-based approaches. We first discuss the development and key limitations of three representative Ising-machine platforms, namely quantum annealers, digital annealers, and coherent Ising machines, which provide the broader context and reference points for evaluating emerging-device-based approaches. We then focus on three major classes of emerging-device-based Ising machines, namely crossbar array-based, stochastic p-bit, and oscillator-based Ising machines, examining how the intrinsic physical and device properties of each platform translate into computational functions, hardware architectures, and system-level performance and scalability. Within this device-to-system framework, we analyze the dominant bottlenecks of each platform, including array nonidealities and peripheral overhead in crossbar-based systems, device variability, reliability, and probability-generation overhead in stochastic p-bit systems, and synchronization and coupling-network complexity in oscillator-based systems. By comparing these platforms within a common device-to-system framework, we identify how distinct physical mechanisms and computational primitives lead to different system-level advantages and scaling constraints. Based on this comparative analysis, we further discuss the requirements for device integration, reliability, coupling and peripheral circuitry, architectural scalability, and system-level benchmarking toward practical Ising-machine hardware. Key challenges in these systems, including sparsity in crossbar-based implementations and delay in oscillator-based architectures, are discussed from this perspective. Finally, we outline future directions toward scalable and energy-efficient Ising machine hardware by emphasizing the importance of physically informed design strategies for bridging device-level physics and system-level optimization performance, thereby enabling physically driven computing paradigms for complex optimization tasks.

2 | Historical Development of Ising Machines

2.1 | Theoretical Foundations of Ising Machines

The concept underlying Ising machines originates from the Ising model, introduced in 1925 by Ernst Ising to describe ferromag-

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netism [24]. The model explains how atomic spins in a solid interact with one another and tend to align in the same direction, resulting in macroscopic magnetization. The Ising Hamiltonian is given by:

$$H = \sum_{i,j=1}^{N} J_{ij}\sigma_i\sigma_j + \sum_{i=1}^{N} h_i\sigma_i \quad (1)$$

where σ_i represents the Ising spin, taking values +1 (up spin) or –1 (down spin). The parameter J_{ij} denotes the interaction strength between spins i and j, and h_i represents the external magnetic field applied to spin i. The ground state of this Hamiltonian corresponds to the minimum-energy configuration of the spin system. Importantly, it was shown in 1982 that finding this minimum-energy configuration is closely related to solving computationally hard combinatorial optimization problems. In particular, Barahona demonstrated that determining the ground state of an Ising system is NP-hard, thereby establishing a fundamental connection between statistical physics and combinatorial optimization [25]. This implies that a wide range of optimization problems can be reformulated as the minimization of the Ising Hamiltonian, where binary decision variables are represented by spins and their pairwise interactions encode the cost function and constraints of the problem.

In parallel with these developments, Hopfield introduced a recurrent neural network model in 1982, known as the HNN, which provided an explicit dynamical system for minimizing an energy function analogous to the Ising Hamiltonian [26]. In this model, symmetric synaptic weights define pairwise interactions between binary neurons, and the network evolves toward stable states corresponding to local minima of the energy landscape. Although originally proposed for associative memory, the HNN established a direct connection between neural computation and energy-based optimization, forming one of the earliest computational realizations of Ising-type dynamics. Following this theoretical connection, Kirkpatrick et al. introduced the concept of SA in 1983, inspired by the physical annealing process in statistical mechanics [17]. They proposed a stochastic optimization method that allows the system to escape local minima by accepting energy-increasing transitions with a probability governed by temperature. As the temperature gradually lowers, the system converges toward a low-energy state, approximating the global optimum of the corresponding energy landscape.

Building upon the deterministic energy minimization of the HNN, the Boltzmann machine, introduced by Ackley et al. in 1985, embeds stochasticity directly into the network dynamics, allowing each unit to update probabilistically according to the Boltzmann distribution [27]. This enables the system not only to escape local minima, as in SA, but also to naturally sample from the energy landscape, providing a principled framework for both optimization and probabilistic inference. As a result, the Boltzmann machine represents a significant conceptual advancement by unifying statistical mechanics and neural computation, where learning and optimization are performed through stochastic dynamics governed by an energy function equivalent to the Ising Hamiltonian. From a physical perspective, these developments collectively highlight how optimization can be interpreted as an energy minimization process governed by stochastic or dynamical transitions in complex state spaces.

In this context, it is important to distinguish the underlying mechanisms of different annealing strategies. While SA relies on thermally activated barrier crossing, where the escape probability increases with temperature by $P \sim \exp(-\Delta E/k_B T)$, quantum annealing exploits quantum tunneling to penetrate energy barriers. This fundamental difference leads to distinct scaling behavior, as tunneling probability depends not only on barrier height but also on barrier width, enabling transitions that are difficult to achieve through purely thermal processes. Quantum annealing, first formulated by Kadowaki and Nishimori in 1998 [25], introduces quantum fluctuations through a transverse-field Ising model. Instead of thermally surmounting energy barriers, the system exploits quantum tunneling to penetrate them, allowing transitions between local minima even at low effective temperatures. This approach extends energy-based optimization from classical stochastic dynamics to quantum mechanical evolution, emphasizing the role of intrinsic physical processes in enabling efficient exploration of complex solution spaces.

2.2 | Comparative Analysis of Hardware Architectures for Ising Machines

The first large-scale realization of an Ising machine was achieved through quantum annealers developed by D-Wave Systems, which physically implement the energy minimization of the Ising Hamiltonian. This approach provides a direct physical mapping between optimization problems and quantum dynamics, enabling energy minimization through intrinsic quantum processes [28]. In 2011, Johnson et al. demonstrated programmable quantum annealing using a superconducting flux qubit system, showing that an artificial Ising spin network can be solved via quantum dynamics [29]. In the same year, D-Wave introduced the D-Wave One system with 128 qubits, representing the first commercially available quantum annealer. The operation of quantum annealers is based on the adiabatic evolution of a time-dependent Hamiltonian. Early studies focused on determining whether the system behavior could be explained by classical stochastic models or required a quantum mechanical description. Subsequent experimental investigations provided strong evidence supporting the quantum nature of the system, including observations of quantum effects in multi-qubit dynamics and quantum correlations [30, 31]. In particular, later studies demonstrated that finite-range quantum tunneling can play a significant role in enhancing optimization performance by enabling transitions through energy barriers that are difficult to overcome via thermal activation [32, 33]. These findings highlight a key advantage of quantum annealing over classical approaches. Following these developments, continuous improvements in hardware architecture have led to substantial scaling of quantum annealers. Boothby et al. introduced the Advantage processor with over 2000 superconducting qubits and improved connectivity [34]. More recently, programmable spin-glass systems exceeding 5000 qubits have been demonstrated, further advancing the capability to solve larger and more densely connected Ising problems [35]. These architectural advancements significantly improve embedding efficiency and scalability, marking an important

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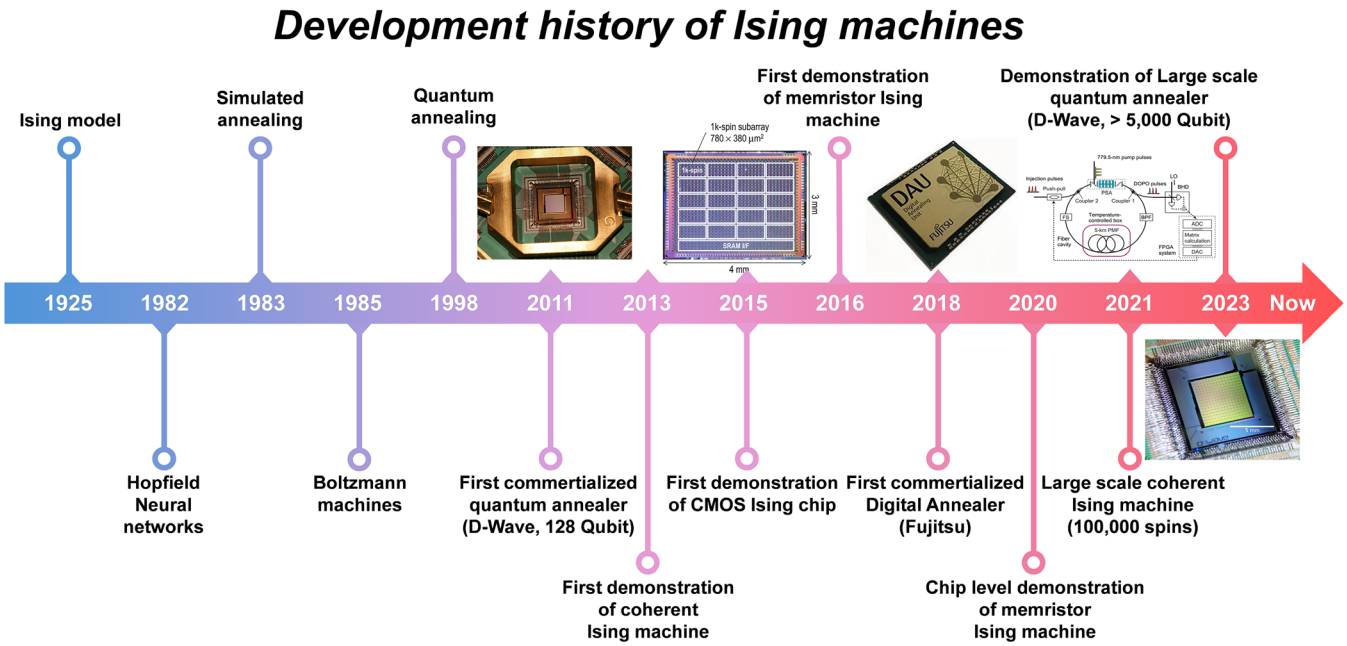

FIGURE 1 | Development history of Ising machines. The evolution of Ising machines is illustrated from early theoretical foundations to large-scale hardware implementations. The Ising model (1925) established the physical basis for spin-based energy minimization, followed by the development of neural and stochastic optimization frameworks, including Hopfield networks (1982), simulated annealing (1983), and Boltzmann machines (1985). The concept of quantum annealing was later introduced, leading to the first commercial quantum annealer (D-Wave system with 128 qubits) and its subsequent scaling to large-scale systems (>5000 qubits). In parallel, hardware implementations of Ising machines have emerged across multiple platforms, including CMOS-based Ising chips, digital annealers, and coherent and oscillator-based Ising machines. Recent advancements focus on large-scale integration and improved computational efficiency, highlighting the convergence of device physics, circuit design, and optimization algorithms toward practical Ising machine realizations.

step toward practical large-scale optimization using quantum annealing. Despite these advancements, quantum annealers face inherent limitations due to their reliance on cryogenic cooling systems and high power consumption [7, 36, 37]. Furthermore, their hardware-specific connectivity constraints, such as the Chimera and Pegasus topologies, restrict the class of problems that can be efficiently embedded and solved [38–40].

In contrast to quantum annealers, relying on quantum mechanical evolution, digital CMOS Ising machines implement Ising optimization using classical digital hardware. These systems aim to emulate the energy minimization dynamics of the Ising Hamiltonian through highly parallel and deterministic or stochastic update rules, typically realized in CMOS-based architectures. One of the earliest hardware implementations of a digital Ising machine was reported by Yamaoka et al. in 2015, which developed a CMOS-based annealing processor capable of handling large-scale optimization problems [41]. In this architecture, Ising spins are represented as binary variables and updated using parallel update rules implemented with standard CMOS logic. This work demonstrated that efficient exploration of the solution space can be achieved using fully digital hardware, establishing a practical pathway for Ising optimization on conventional semiconductor platforms. Building on this approach, Fujitsu developed the digital annealer, a commercially successful large-scale optimization system based on CMOS technology [42, 43]. It employs a modified SA algorithm with massively parallel trial updates and efficient cost-function evaluation, enabling rapid convergence for large-scale problems. A key advantage of the digital annealer is its ability to support fully connected interactions between spins, thereby eliminating the need for minor embedding, which is a significant computational bottleneck in quantum annealers with limited connectivity. This allows efficient handling of dense optimization problems without additional mapping overhead. However, since the system relies on stochastic update rules, additional circuit overhead is required to generate randomness (e.g., random number generators), which can impact overall hardware efficiency [44–46]. Beyond RNG overhead, the fully connected architecture also requires the storage and processing of a dense coupling matrix whose size increases approximately as $O(N^2)$, increasing memory-capacity requirements and memory-access bandwidth as the problem size grows. When the system is scaled across multiple processing units or chips, communication of spin-state information can impose substantial inter-chip bandwidth overhead, introducing an additional architectural bottleneck. The achievable degree of parallel spin updating also depends on the hardware architecture and update scheme, while finite coupling-coefficient precision can limit the accurate representation of the target Hamiltonian. In addition, the implementation of annealing schedules introduces trade-offs among convergence behavior, solution quality, and computational latency. Consequently, the scalability and efficiency of digital annealers depend not only on random-number generation but also on memory organization and bandwidth, interconnect communication, update parallelism, numerical precision, and algorithm–hardware co-design.

Coherent Ising machines (CIMs) represent an alternative class of Ising solvers that exploit optical coherence and nonlinear

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TABLE 1 | Comparison of representative Ising-machine platforms in terms of spin representation, interaction scheme, demonstrated scale, connectivity, key implementation challenges, and demonstration level.

	D-Wave	Coherent Ising Machine	CMOS annealer	Crossbar array-based Ising machine*	Stochastic p-bit Ising machine*	Oscillator-based Ising machine
Spin representation	Qubit	Optical pulse / phase	Digital binary state (register / memory)	CMOS neuron	Probabilistic bit	Oscillator phase
Interaction scheme	superconducting coupler	Optical / electronic feedback	Digital coupling circuit	Memristor crossbar	Digital coupling (FPGA / ASIC)	Resistor / capacitor / transmission gate
Representative demonstrated spin scale	>5000	>100 000	8192	60	1143	1968
Connectivity	Sparse	All-to-all	All-to-all	All-to-all	Sparse	Sparse
Representative hardware	Superconducting quantum annealer	DOPO, OEPO	Digital annealer	Memristor	MTJ / memristor	CMOS ring / LC / biristor / IMT
Key implementation challenges	Cryogenic operation, noise sensitivity	Noise sensitivity, feedback latency	RNG requirements, digital circuit overhead	Peripheral interface overhead, large-scale array nonidealities	Peripheral interface overhead, D2D/C2C variation, reliability	Synchronization, coupling-network complexity
Demonstration level	Commercial	Large-scale system demonstration	Commercial	Small-scale system demonstration	Small-scale system demonstration	Small-scale system demonstration

*Hybrid implementations combining stochastic p-bits with crossbar-based coupling are also possible.

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dynamics to perform energy minimization. Unlike digital and quantum annealers, which rely on discrete updates or quantum evolution, CIMs utilize continuous-time dynamics of optical systems to emulate the Ising Hamiltonian. The concept was first proposed by Yamamoto et al. in 2011, mapping Ising spins onto the phase states of injection-locked laser systems [47]. The first experimental realization of a CIM was reported by Wang et al. in 2013 using degenerate optical parametric oscillators (DOPOs) [48]. This approach was significantly advanced by Inagaki et al. in 2016, demonstrating a scalable CIM capable of solving optimization problems with up to 2000 spins [49]. In this system, each DOPO encodes an Ising spin in its phase (0 or π), and a large number of spins are represented using time-multiplexed optical pulses circulating in a fiber loop. The interaction matrix is implemented via a measurement-feedback scheme, where optical signals are partially extracted, processed electronically to compute weighted sums according to the coupling coefficients J_{ij}, and reinjected into the system. This enables programmable all-to-all connectivity between spins. The system evolves through nonlinear gain and loss dynamics, and as the pump power increases, a bifurcation process drives each oscillator to one of the two phase states, guided by mutual coupling toward low-energy configurations [15, 50–53]. More recently, CIMs have demonstrated remarkable scalability. Honjo et al. reported a 100 000-spin CIM using time-multiplexed pulses in kilometer-scale fiber loops, highlighting the potential of optical platforms for large-scale combinatorial optimization [54]. However, such large-scale measurement-feedback CIMs require substantial hardware resources for long optical cavities, stabilization, measurement, and FPGA-based coupling computation, resulting in significant hardware overhead [33]. Beyond conventional optical CIMs, related time-multiplexed Ising machines have also been realized using optoelectronic feedback and microwave-domain oscillators [55, 56]. These approaches can alleviate some of the constraints associated with conventional fiber-cavity implementations by employing alternative spin-encoding and feedback mechanisms. Nevertheless, the scalability of CIMs and related time-multiplexed Ising machines is determined by a broader range of optical, electronic, and architectural factors rather than by cavity length alone. Measurement-feedback implementations require high-speed detection, ADC/DAC interfaces, and electronic matrix multiplication to realize programmable spin interactions, introducing additional communication, latency, and energy overhead. Optical loss and noise can further affect signal integrity and spin stability, while flexible connectivity and programmability may require increasingly complex feedback and coupling schemes. In addition, problem-mapping and embedding requirements and the integration of optical and electronic components remain important considerations for translating large spin counts into practical optimization hardware. Therefore, although CIMs have demonstrated substantial scalability in terms of spin count, translating this scale into hardware-efficient optimization systems requires the co-design of optical dynamics, programmable coupling, feedback electronics, and system-level integration.

Another important class of Ising machines is based on in-memory computing architectures. Memristor devices have attracted significant attention in this context due to their ability to perform matrix–vector multiplication efficiently in crossbar arrays, enabling analog in-memory computation [57–60]. The first in-memory computing-based Ising machine was reported in 2016, where combinatorial optimization problems were mapped onto hardware using resistive crossbar arrays [61]. Subsequently, a chip-level experimental demonstration was reported in 2020, establishing the feasibility of memristor-based HNNs for hardware Ising optimization [62]. These systems are typically based on the HNN framework, where spin variables are stored externally, while the interaction matrix is mapped onto the memristor crossbar in the form of an adjacency matrix. The system evolves according to energy minimization dynamics, often incorporating noise to emulate SA behavior. Such architectures are commonly referred to as mem-HNNs. Although they originate from neural network formulations, they fall within the category of Ising machines, as they solve combinatorial optimization problems through the minimization of an Ising-equivalent energy function [13]. This relation highlights the close connection between neural network-based computation and physics-driven optimization. Recent research in this area can be broadly categorized into two directions. The first focuses on implementing spin update dynamics directly within device physics to reduce external computational overhead. The second aims to exploit and control intrinsic device noise within crossbar arrays to realize hardware-level annealing processes. These approaches will be discussed in more detail in the following section.

Finally, another emerging class of Ising machines is based on dynamical annealing using coupled oscillator systems. In these approaches, the Ising problem is solved through the collective dynamics of interacting oscillators, where the system evolves toward a low-energy configuration via phase synchronization. The foundational framework of oscillator-based Ising machines is often built upon LC oscillators, where phase differences between oscillators encode Ising spins, and coupling between oscillators implements the interaction matrix [19]. Such systems naturally perform energy minimization through continuous-time dynamics, providing an alternative to discrete or stochastic update-based methods. More recent studies have explored the use of emerging devices to realize compact and energy-efficient oscillator-based Ising machines. For instance, insulator–metal transition (IMT) materials such as VO_2 have been utilized to implement relaxation oscillators with intrinsic nonlinear dynamics, enabling hardware-level realization of coupled oscillator networks for combinatorial optimization [21]. Similarly, bistable devices such as biristors, originally demonstrated in silicon nanowire structures, have been employed to construct coupled oscillatory systems, where their inherent nonlinear switching dynamics can be exploited for Ising-like optimization [20]. These approaches share a common principle: instead of explicitly computing energy updates, the system leverages intrinsic device and circuit dynamics to naturally evolve toward energy-minimizing states. From this perspective, oscillator-based systems can be regarded as dynamical Ising machines, as they solve combinatorial optimization problems through physical evolution governed by nonlinear dynamics. Further discussions on these approaches are provided in the following section. Figure 1 summarizes the historical development of Ising machines.

Overall, these hardware implementations of Ising machines exhibit fundamentally different trade-offs in terms of scalability, connectivity, energy efficiency, and implementation complexity. Quantum annealers offer direct physical realization of the Ising Hamiltonian with potential advantages in exploring complex

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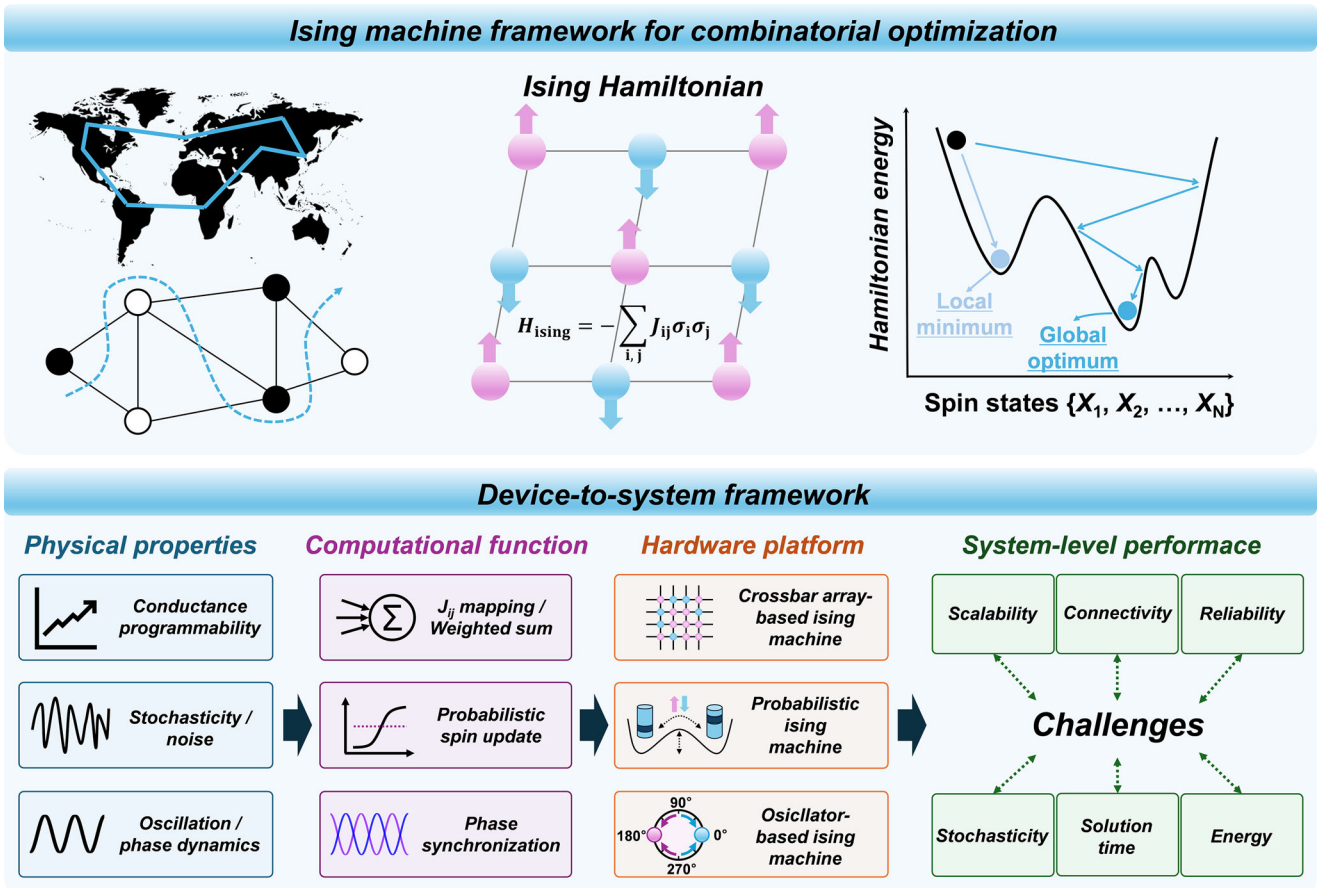

FIGURE 2 | Device-to-system framework of Ising machines. The upper panel illustrates the general optimization process, where a combinatorial optimization problem is mapped onto an Ising Hamiltonian by encoding decision variables as spins and problem constraints as spin interactions. The spin states are then iteratively evolved toward lower-energy configurations, with the minimum-energy state corresponding to the optimal or near-optimal solution. The lower panel summarizes the device-to-system relationships among physical properties, computational functions, and representative hardware platforms, including crossbar array-based, probabilistic, and oscillator-based Ising machines. The resulting system-level characteristics are evaluated in terms of scalability, connectivity, reliability, stochasticity, solution time, and energy.

energy landscapes, but they are constrained by cryogenic operation and limited connectivity. Digital annealers provide high flexibility and full connectivity based on mature CMOS technology, yet they incur significant overhead in stochastic number generation and energy consumption. CIMs enable fast and highly parallel computation through optical dynamics, although large-scale implementations often require substantial optical, measurement, feedback, and digital processing hardware. These trade-offs indicate that no single architecture is universally optimal, and that application-specific co-design across materials, devices, circuits, and algorithms is essential for realizing practical and scalable Ising machine hardware. From this perspective, the performance of Ising machines is fundamentally governed by the interplay between physical dynamics and system-level design constraints. Table 1 compares representative Ising-machine platforms in terms of spin implementation, interaction scheme, demonstrated scale, connectivity, key challenges, and demonstration level. This comparison places the three emerging-device-based approaches discussed in the following sections, namely crossbar array-based, probabilistic p-bit, and oscillator-based Ising machines within the broader Ising-machine landscape. Figure 2 summarizes the device-to-system framework adopted throughout this review, linking intrinsic physical properties of emerging devices to their computational functions, representative hardware architectures, and system-level characteristics. Within this framework, conductance programmability, stochastic device dynamics, and oscillation and phase dynamics provide distinct physical primitives for interaction-weight mapping and weighted summation, probabilistic spin updates, and synchronization-based computation, respectively. The following sections therefore examine crossbar-based Ising machines, stochastic p-bit Ising machines, and oscillator-based Ising machines from this device-to-system perspective, with particular attention to how their underlying physical mechanisms influence scalability, connectivity, reliability, solution time, and energy efficiency.

3 | Emerging Device-Based Ising Machines for Combinatorial Optimization

3.1 | Crossbar Array-Based Ising Machines

Among the representative approaches for implementing Ising solvers, stochastic neural network–based methods have attracted considerable attention. In particular, the Boltzmann machine can be regarded as a probabilistic extension of the HNN, in which

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binary neuron states evolve according to an energy function equivalent to the Ising Hamiltonian in Equation (1) [26, 27]. This formulation provides a natural bridge between statistical physics–based optimization and hardware implementations of stochastic computing. In contrast, conventional HNNs exhibit deterministic dynamics that generally evolve toward lower-energy stable states, making them prone to becoming trapped in local minima. To overcome this limitation, annealing methods inspired by statistical mechanics enable probabilistic exploration of the energy landscape, allowing the system to approach the global minimum. This process is known as SA [17, 63, 64]. In thermal equilibrium, a classical physical system follows the Boltzmann distribution given by

$$P_n = \frac{exp\left(-\frac{E_n}{k_B T}\right)}{Z} \tag{2}$$

where $Z = \sum_n \exp(-\frac{E_n}{k_B T})$, k_B is the Boltzmann constant, and T is the thermodynamic temperature, and E_n denotes the energy of state n as defined in Equation (1). Based on this distribution, the state evolution follows a temperature-dependent probabilistic update rule, typically described by a sigmoid activation function. The probability of spin flipping is determined by the energy change ΔE, where transitions reducing the system energy are more likely to occur, while energy-increasing transitions can still occur with a finite probability. SA is implemented by gradually lowering the temperature, which effectively sharpens the sigmoid function. As the temperature decreases over iterations, the probability of accepting energetically unfavorable updates is reduced, allowing the system to avoid local minima and converge toward low-energy states.

Meanwhile, HNN–based Ising machines are particularly well suited for hardware implementation, especially in crossbar array architectures using memory devices [16, 65–68]. Their operation is dominated by repeated weighted summation defined by an interaction matrix, which can be efficiently mapped onto physical hardware. A crossbar array is a structure composed of two-terminal devices arranged between orthogonal word lines (WLs) and bit lines (BLs). Memory devices, including resistive or capacitive elements, are located at each intersection of WL and BL, enabling parallel read and write operations [69–73]. When input voltages are applied to the WLs, currents proportional to the device conductance are generated at each cross point according to Ohm's law. These currents are then summed along the BLs following Kirchhoff's current law, resulting in weighted summation operations. Based on this operating principle, crossbar arrays naturally implement vector matrix multiplication (VMM). Owing to their simple structure, high integration density ($4F^2$), and efficient parallel computation capability, crossbar arrays have been widely investigated as a promising platform for in-memory computing, where computation within the memory array can reduce data-movement overhead, a major bottleneck in conventional von Neumann architectures [74–84]. This direct physical realization of VMM is a key enabler for scalable hardware Ising solvers.

Based on this framework, Ising problems can be mapped onto a crossbar array structure, as shown in Figure 3a, by encoding the adjacency matrix into device conductance and representing spin states as input voltages. The resulting local field can be expressed as follows:

$$I_i = \sum_{j=1}^{N} G_{ij} V_j + I_i^b \tag{3}$$

and the corresponding energy can be expressed as:

$$E = -\sum_{i=1}^{N} V_i I_i, \tag{4}$$

where V_{i} represents the binary input vector, I_{i} is the output current, $I_{\mathrm{i}}{}^{\mathrm{b}}$ is the bias current, and G_{ij} denotes the synaptic weight. Therefore, the input vector is applied to the array as voltages, and the resulting summed current is used to compute the system energy [85]. The input vector is then updated in the direction that reduces the energy, and the updated vector is reapplied to the array. This iterative process is repeated until the system converges to a low-energy state. To avoid being trapped in local minima and to approach the global minimum of the energy function, SA is employed by controlling the effective temperature, as discussed earlier. As illustrated in the right panel of Figure 3a, this can be implemented in crossbar arrays by introducing controllable noise into the VMM operation. Such noise may originate from the inherent stochasticity of the devices, external measurement noise, or intentionally injected noise through peripheral circuits. At the initial stage, a high noise level increases the probability of spin flipping, enabling exploration of the energy landscape. As the iterations proceed, the effective temperature is gradually reduced by decreasing the noise level, which suppresses unnecessary state transitions and promotes convergence toward low-energy states. This mechanism establishes a direct correspondence between noise characteristics in hardware and temperature scheduling in SA.

One representative implementation of Ising machines using crossbar arrays is based on memristive devices, particularly resistive random access memory (RRAM), where VMM is combined with the intrinsic stochasticity of the devices to realize SA. In RRAM devices, electrons are randomly captured and emitted by trap sites within the device, leading to current fluctuations known as random telegraph noise (RTN) [86–90]. In addition to RTN, other noise sources such as $1/f$ noise and thermal noise can also contribute to the overall stochastic behavior of the device [91–93]. This stochastic behavior results in temporal variations in the read current, which is typically considered undesirable for conventional memory operation. However, such intrinsic noise can be effectively exploited to implement the stochastic dynamics required for SA, representing a paradigm shift from suppressing noise to actively utilizing it for computation [94, 95]. In practical implementations, the effective temperature can be controlled by adjusting the signal-to-noise ratio (SNR) of the readout current. Since the output current scales with the applied read voltage while the noise level remains relatively independent of it, the SNR can be modulated by tuning the read voltage, enabling a simple yet effective way to control the annealing schedule in hardware [85, 96–99]. Mahmoodi et al. experimentally demonstrated SA based on an RRAM crossbar array by utilizing SNR control in 2019 [99]. As shown in Figure 3b, a 64 × 64 0T1R crossbar array was fabricated, along with the corresponding device cross-section.

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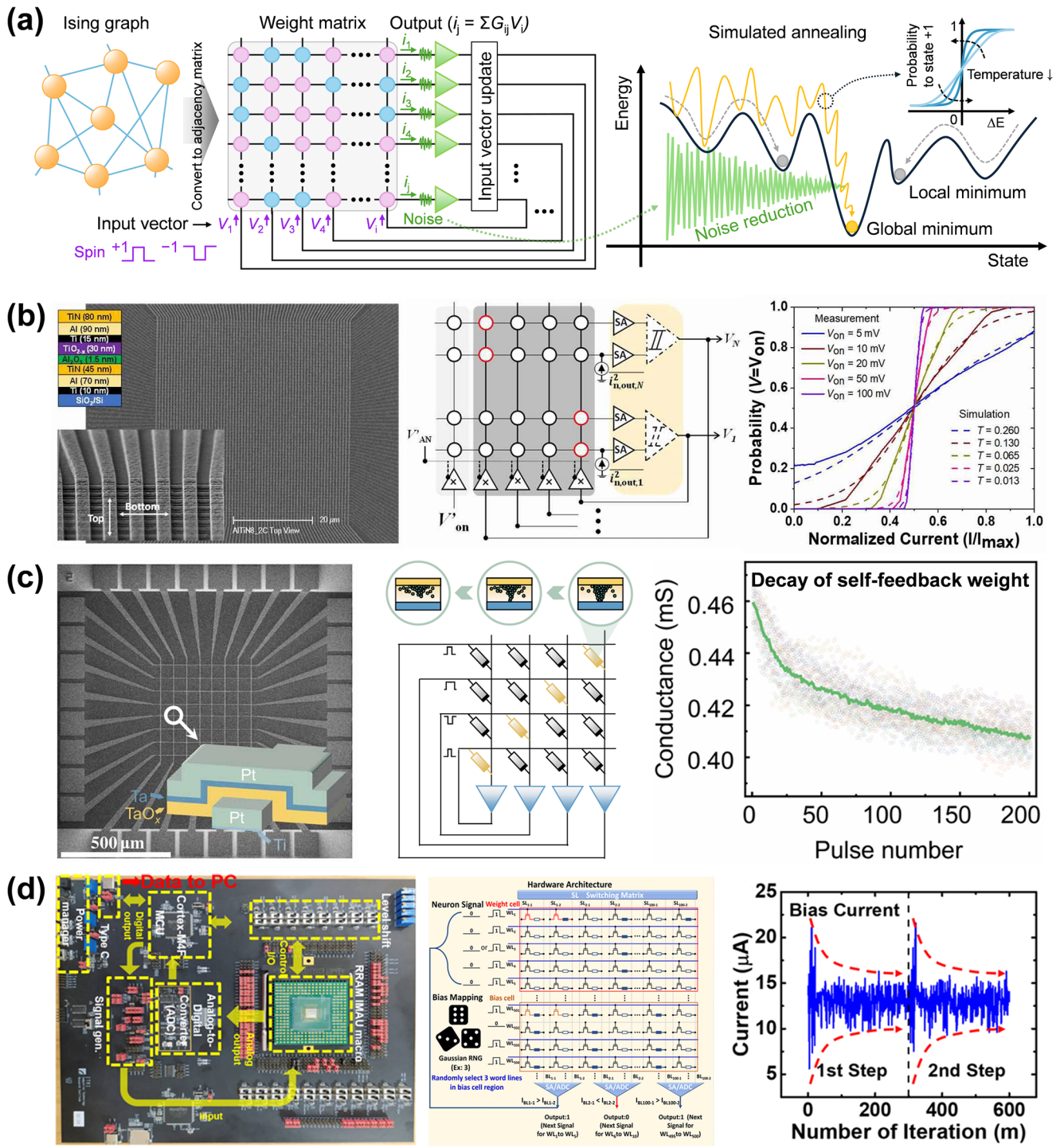

FIGURE 3 | Crossbar array-based Ising machines. (a) Conceptual illustration of mapping an Ising optimization problem onto a crossbar array, where the graph is converted into an adjacency matrix and encoded as device conductances, and spin states are applied as input vectors to enable VMM-based computation (left panel). The outputs are iteratively updated to minimize the system energy, while SA is implemented by gradually reducing noise, enabling convergence from local minima to the global minimum (right panel). (b) SEM image of the fabricated 64 × 64 0T1R memristor crossbar array and device cross-section (left panel), circuit diagram for stochastic SA (middle panel), and measured probabilistic sigmoid function controlled by read-voltage–dependent SNR, compared with the ideal sigmoid (right panel). Reproduced with permission [99]. Copyright 2019, IEEE. (c) SEM image of the Ta/TaO_x/Pt memristor crossbar array and device schematic (left panel), mapping onto a Hopfield network where diagonal devices act as self-feedback weights enabling transient chaotic dynamics via progressive resetting, while others encode constant synaptic weights (middle panel), and conductance evolution of diagonal devices showing double-exponential decay under identical programming pulses (right panel). Reproduced with permission [104]. Copyright 2020, American Association for the Advancement of Science. (d) Photograph of the PCB test board for the 1152 × 1024 1T1R RRAM-based IMAU chip (left panel), hardware mapping using RRAM pair cells with stochastic annealing via randomly activated bias cells (middle panel), and measured current evolution exhibiting dynamically decaying bias-induced noise (right panel). Reproduced with permission [106]. Copyright 2021, IEEE.

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The middle panel illustrates the schematic of the proposed neuro-optimization hardware, where each neuron is implemented using the crossbar array together with two sense amplifiers and a comparator. In this architecture, vector matrix multiplication in the crossbar array is combined with controllable SNR through adjustment of the read voltage. The noise of the summed current arises from both the memory devices along the differential lines and the peripheral sensing circuits. The readout current is fed into a comparator, which converts the analog current into a probabilistic digital output. Specifically, the probability of latching a digital high state follows $0.5(1+\mathrm{erf}(\frac{I}{\sqrt{2}\sigma}))$, where σ is the standard deviation of the output current. This probabilistic response approximates a sigmoid activation function, enabling stochastic neuron behavior. The output voltage is then updated and reapplied to the array input for the next iteration. Since the readout current is proportional to the applied voltage, while the noise is largely independent of it, the SNR increases with increasing read voltage, with the maximum SNR given by $\mathrm{SNR}_{\max} = I_{\max}/\sigma$. As shown in the right panel of Figure 3b, the probabilistic sigmoid function can be experimentally modulated by adjusting the read voltage, which controls the SNR. This provides a simple and effective way to implement temperature control for SA in hardware. Using this approach, the system was applied to a 10-node weighted graph partitioning problem, and the network was shown to reach the ground state at earlier epochs compared to baseline methods. In addition to pairwise interactions, crossbar-based Ising machines can also incorporate local bias terms through dedicated bias conductance. Mahmoodi et al. demonstrated such an approach in a floating-gate memory-based neuro-optimization system, where the neuron input was represented by the weighted sum of synaptic currents and an additional bias current [85]. In the hardware architecture, the pairwise synaptic weights were mapped to the main memory array, while the bias contribution was implemented using dedicated conductances connected through a separate bias line. The synaptic and bias currents were then summed at the neuron input, enabling both the pairwise interaction and local bias terms to be directly incorporated into the memory-based computation. In their adjustable neuro-optimization scheme, an additional node was introduced to modify the energy landscape. This node was implemented by extending the original memory-cell array by one row and one column, together with an additional bias line to distinguish the bias-current contribution associated with the added node. These results demonstrate that local bias terms can be incorporated into memory-based crossbar computation together with pairwise interactions. However, depending on the implementation, dedicated bias conductance, additional memory cells, and interconnect resources can increase array and routing overhead. Therefore, the hardware cost associated with both pairwise interactions and local bias terms should be considered when evaluating the scalability of crossbar-based Ising machines.

A key design consideration in crossbar-based Ising machines is the trade-off between stochastic exploration and computational precision. Intrinsic and externally injected noise play a crucial role in enabling probabilistic state transitions, allowing the system to escape local minima and explore the energy landscape effectively. However, excessive noise can degrade the fidelity of the weighted summation operation and lead to incorrect or unstable convergence. Conversely, reducing noise improves computational accuracy but increases the risk of the system being trapped in suboptimal local minima. Therefore, achieving an optimal balance between noise-induced exploration and deterministic convergence is essential for reliable operation. This balance can be typically controlled through parameters such as read voltage, bias current, or peripheral noise injection, which effectively modulate the signal-to-noise ratio and emulate temperature scheduling in hardware-level annealing processes.

Another approach to implementing Ising machines using crossbar arrays is based on chaotic simulated annealing (CSA), where transient chaos is introduced into an HNN [64, 100–102]. In this approach, self-feedback weights are incorporated into the network and gradually reduced during iterations, enabling a transition from chaotic dynamics to convergence and facilitating escape from local minima [68, 85, 99, 103, 104]. Yang et al. demonstrated such a CSA scheme in 2020 by exploiting the intrinsic nonlinear weight decay characteristics of memristor devices [104]. Figure 3c illustrates the mapping of the memristor array onto a Hopfield network, where the diagonal devices represent self-feedback weights responsible for transient chaotic dynamics, while the remaining devices encode constant synaptic weights. The self-feedback weights are progressively reduced by programming the diagonal devices, enabling the transition from chaotic exploration to stable convergence. Specifically, during each iteration, depression pulses are applied to the diagonal memristors to gradually decrease their conductance, which corresponds to the update rule $z_i\,(t+1) = (1-\beta)z_i(t)$, where z_i denotes the self-feedback weight of neuron i, t represents the iteration step, and β is the damping parameter. The self-feedback weights can be reduced following arbitrary annealing functions such as linear or exponential decay. These decay behaviors were implemented by modulating the number and width of programming pulses applied to the memristor devices. The right panel of Figure 3c shows the conductance modulation of the Ta/TaO_x/Pt device under identical programming pulses of −1.25 V and 2 µs, where the averaged response is well fitted by a double exponential decay function. Yang et al. further conducted simulations on 10 randomly generated city graphs, with each graph evaluated over 100 different initial conditions. The results show that both exponential and long-term depression annealing achieve higher probabilities of reaching the global optimum with fewer iteration cycles, and further validate that combinatorial optimization problems can be effectively solved by exploiting transient chaotic dynamics through the gradual resetting of memristor devices. However, this device-driven annealing scheme also introduces several practical challenges. Since the self-feedback weights are gradually reduced through repeated programming of the diagonal memristors during optimization, frequent conductance updates may increase write energy and latency while also raising endurance concerns, particularly for large-scale problems requiring many iterations. Moreover, the annealing trajectory depends directly on the intrinsic conductance-decay characteristics of the memristor devices. Therefore, device-to-device variation or temporal changes in the programming characteristics could lead to nonuniform annealing rates across neurons, potentially perturbing the intended transient chaotic dynamics and degrading optimization performance as the system scales.

Finally, another approach to implementing crossbar-based hardware Ising machines is to incorporate controllable stochasticity at

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the circuit and system level, rather than relying solely on intrinsic device noise. In this framework, randomness is introduced into the computation through additional circuitry, such as bias currents and peripheral control, and is dynamically regulated during iterations to realize SA [62, 105, 106]. Hong et al. demonstrated such an approach by utilizing additional stochastic bias currents in an RRAM-based in-memory annealing unit (IMAU) [106]. Figure 3d shows a photograph of the PCB test board for the IMAU chip based on a 1152 × 1024 1T1R RRAM array and illustrates the hardware mapping, where synaptic weights are encoded using RRAM cell pairs, and SA is implemented via randomly activated bias cells. Specifically, stochastic bias currents are injected through additional bias cells placed on the BLs, which are randomly activated via the WL decoder following a Gaussian distribution. The accumulated bias current is added to the MAC output and gradually reduced over iterations, enabling controllable noise injection for annealing. The right panel of Figure 3d shows the measured current changes, demonstrating dynamically decaying noise generated from the bias currents during the annealing process. Furthermore, a multi-step SA scheme is employed, in which multiple annealing cycles are sequentially performed with intermediate updates of the solution, allowing progressive refinement of the system state. Using this approach, a 10-city traveling salesman problem was successfully solved, where the multi-step SA converges to the shortest possible route. This work demonstrates a hardware–algorithm co-designed in-memory annealing unit that effectively solves combinatorial optimization problems by embedding stochastic bias-based annealing directly within the crossbar array. However, embedding stochasticity directly into the array introduces additional hardware mapping overhead. In particular, multiple RRAM cells may be required to represent multilevel weights, while additional bias cells must be allocated for stochastic annealing, increasing the number of physical cells required for each logical interaction and reducing the effective array utilization. Consequently, the scalability benefit of in-array stochasticity should be evaluated together with the additional cell and array resources required for its hardware implementation.

Beyond these hardware implementations, the performance of crossbar-based Ising machines relative to conventional digital platforms has also been quantitatively evaluated at the system level. Cai et al. compared the projected performance of a memristor-based HNN with an NVIDIA GeForce GTX 1080 Ti GPU running a noisy mean-field annealing algorithm for a dense 60-node Max-Cut benchmark [62]. The parallel mem-HNN achieved a projected time-to-solution of 600 ns, compared with 10 μs for the GPU, corresponding to an approximately 17-fold reduction in solution time. In addition, the estimated energy-to-solution was 72 nJ for the mem-HNN, compared with an upper-bound estimate of 2.5 mJ for the GPU. Although this comparison reflects complete Ising-solver implementations rather than an isolated VMM-kernel benchmark, it illustrates the potential system-level benefits of analogue in-memory VMM, where highly parallel weighted accumulation is performed directly within the crossbar array while reducing repeated data movement between memory and processing units. However, the speed and energy advantages are specific to the benchmark considered and may not universally hold across different problem sizes, graph topologies, mapping strategies, and hardware configurations.

Despite these advantages in computational speed and energy efficiency, crossbar-based Ising machines still face several challenges that limit their scalability and practical implementation. One major limitation arises from the rapid increase in the required memory-array size as the problem scale increases. For example, direct mapping of an N-node dense Max-Cut problem requires an $N \times N$ interaction matrix, corresponding to $O(N^2)$ weight storage. The mapping overhead becomes even more severe for problems such as the traveling salesman problem (TSP), where an N-city problem requires N^2 spins, resulting in up to $O(N^4)$ interaction-weight storage for a direct dense mapping [98]. As the required crossbar dimension increases, electrical nonidealities such as line resistance, IR drop, and sneak-path currents become increasingly significant, resulting in deviations from the intended VMM operation [107, 108]. Although access transistors in 1T1R arrays can suppress unintended current paths and improve cell selectivity, the increased cell area reduces integration density, introducing another trade-off for large-scale implementations. Large interaction matrices may therefore need to be partitioned across multiple arrays or subarrays, which can mitigate array-level electrical nonidealities but introduces additional routing, accumulation, and inter-array communication overhead. Therefore, improving scalability requires not only device- and circuit-level optimization but also more efficient problem-mapping strategies. Approaches such as hierarchical problem decomposition, sparse interaction mapping, and matrix compression can reduce the number of spins and interaction weights that need to be physically stored and processed in the crossbar array [98, 105]. Such mapping and compression approaches can alleviate the array-size and routing overhead associated with direct mapping, although their effectiveness depends on the problem structure and mapping strategy.

Another challenge arises from mapping the interaction weights onto physical memory states. Because physical conductance is inherently nonnegative whereas Ising coupling coefficients can take both positive and negative values, signed interactions generally require differential conductance mapping, reference cells, or equivalent encoding schemes. These approaches can increase the number of memory cells, sensing complexity, and peripheral-circuit overhead required to represent the interaction matrix. Device-to-device variation, limited conductance precision, and nonlinear or asymmetric programming characteristics can further introduce deviations between the target and physically implemented weight matrices, thereby distorting the intended energy landscape [75]. Achieving high-precision multilevel weights requires tight conductance control and may involve repeated program-and-verify operations, which increase programming latency and energy consumption [109]. Moreover, reconfiguring the crossbar array for different problem instances requires repeated write operations, which can gradually consume the limited endurance of memory devices. Even after programming, retention loss and conductance drift can alter the stored weight values over time, potentially degrading computational accuracy. Therefore, the design of crossbar-based Ising machines should consider not only nominal device characteristics but also the combined effects of programming variability, conductance precision, endurance, retention, and drift on the accuracy and reliability of the physically implemented energy landscape.

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Beyond the memory devices themselves, peripheral circuits often constitute a substantial portion of the total area and energy consumption in crossbar-based hardware systems [110, 111]. Depending on the architecture, practical implementations may require digital-to-analog converters (DACs) and analog-to-digital converters (ADCs), together with switching, multiplexing, sensing, and control circuits. Higher computational precision generally requires higher-resolution data-conversion and sensing circuitry, increasing the associated area, latency, and energy overhead. In addition, hardware annealing schemes may require additional circuitry to control read voltages, modulate noise, generate stochastic bias currents, or implement nonlinear activation functions, as discussed above. Therefore, reducing peripheral-circuit overhead, together with exploiting intrinsic device dynamics wherever possible, is important for preserving the density and energy-efficiency advantages of emerging-device-based Ising machines. Additional design challenges associated with emerging-device-based Ising machines are discussed in more detail in Section 4. Table 2 summarizes representative crossbar array-based Ising machines, providing a comparative overview of their hardware implementations, annealing strategies, interaction-weight precision, stochasticity implementation, and system-level performance.

3.2 | Stochastic Spin Dynamics-Based Ising Machines

Among various efforts toward hardware implementation of Ising machines using emerging devices, probabilistic computing based on stochastic binary units, which exploit intrinsic stochastic spin dynamics of physical devices, has emerged as a promising direction due to its scalability. In particular, such approaches enable direct hardware realization of stochastic state transitions, which are essential for escaping local minima and exploring complex solution spaces. Specifically, Camsari et al. introduced the concept of a p-bit as a tunable stochastic unit representing an unstable element whose output fluctuates between binary states, with switching probabilities governed by a sigmoidal function of its input [112]. As illustrated in Figure 4a, the p-bit represents an intermediate computing paradigm bridging deterministic digital bits and quantum bits through stochastic state evolution [113–116]. Although this behavior can be implemented using CMOS circuits, these implementations typically require additional peripheral circuitry, including digital-to-analog converters, lookup tables, and calibration units, leading to substantial overhead in area, power, and complexity, particularly at large scales. Moreover, stochasticity and nonlinear activation must be externally implemented rather than arising intrinsically from device physics, limiting efficiency and scalability [117, 118]. To address these challenges, stochastic nanomagnets based on magnetic tunnel junctions (MTJs) have emerged as one of the most representative emerging device platforms for realizing p-bits. Unlike conventional memory devices relying on high energy barriers for non-volatile data retention, reducing the energy barrier enables MTJs to operate as stochastic elements, where the magnetization undergoes thermally driven random switching, as shown in Figure 4b. In such stochastic MTJs (sMTJs), the magnetization spontaneously fluctuates between parallel (P) and antiparallel (AP) states at ambient temperature, providing a compact and energy-efficient entropy source. Moreover, the time-averaged magnetization of low-barrier nanomagnets naturally follows a sigmoidal response to input stimuli such as spin current, enabling direct physical implementation of probabilistic activation functions. By exploiting these intrinsic magnetization dynamics, sMTJs can realize p-bit functionality without the need for complex external random number generation circuitry, making them attractive building blocks for scalable stochastic Ising machines [119, 120]. Depending on their operating mechanisms, MTJ-based p-bits can be broadly classified into spin-transfer torque (STT)-based sMTJ implementations [121–129] and spin–orbit torque (SOT)-based sMTJ implementations [130–134].

Camsari et al. demonstrated in 2017 that a p-bit can be implemented using a conventional embedded MRAM structure by integrating a low-barrier MTJ [130, 131]. Figure 4c shows the device structure of the embedded MRAM-based p-bit, realized by modifying a conventional 1T–1MTJ STT-MRAM cell in which the free layer of the MTJ is engineered as a low-barrier magnet. The stochastic switching of the low-barrier magnet provides intrinsic randomness, while the transistor enables controllable probabilistic behavior, achieving functionality equivalent to a three-terminal p-bit. The SPICE simulation results show the output voltage as a function of the input voltage swept from −0.4 to 0.4 V, with the time-averaged response following a sigmoidal (tanh) function. Furthermore, by interconnecting MTJ-based p-bits using a resistor-network crossbar architecture, the authors demonstrated the implementation of Boolean logic, including invertible operations such as an AND gate.

Yang et al. proposed a superparamagnetic tunnel junction (SP-MTJ)–based p-bit by engineering a conventional STT-MRAM structure with an ultrathin Mo insertion layer to enable intrinsic stochastic switching [129]. Figure 4d illustrates the energy barrier comparison between conventional MTJs and Mo-engineered SP-MTJs, showing that the Mo insertion reduces the energy barrier below ∼15 kT, thereby enabling thermally activated stochastic switching. The duty cycle of the SP-MTJ with 1.5 Å Mo insertion exhibited a Poisson-like distribution as a function of the external magnetic field, confirming its stochastic switching behavior. Furthermore, the device characteristics were mapped onto stochastic neuron models in a discrete HNN to solve a 7-city traveling salesman problem, demonstrating improved convergence and enhanced capability to escape local minima compared to deterministic implementations. These results demonstrate the feasibility of exploiting intrinsic SP-MTJ stochasticity for hardware Ising computation without additional randomness-generation circuitry. Zhang et al. demonstrated an Ising computer based on an SOT-MTJ p-bit array in 2025, employing a successive probability approach to extend the computational capability of 1-bit quantization [135]. Figure 4e shows the MTJ stack structure along with SEM, optical, and TEM images of the fabricated device. An Ising computer composed of an 8×2 SOT p-bit array was implemented, and the circuit architecture of each p-bit integrates reading and writing circuits to receive control signals from an MCU and generate SOT-driven stochastic outputs. The right panel of Figure 4e presents the measured switching probability as a function of input voltage, showing deviations from the ideal sigmoidal response and motivating the use of 1-bit quantization. By controlling the bias, the switching probability of SOT p-bits can be continuously modulated, allowing a transition from stochastic to strongly biased states,

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TABLE 2 | Comparison of representative crossbar-based Ising machines in terms of hardware implementation, demonstrated scale, optimization task, annealing method, weight precision, and stochasticity implementation.

Reference	Representation of interaction	Physical entropy source	Demo complexity	Exp./ Sim.	CMOS compatibility	Annealing method	Problem type	Problem scale	Connectivity	Weight precision	Endurance	Stochastic generator	Energy to solution	Time to solution	Power
IEDM 2018 [143]	RRAM + CBRAM	Stochastic CBRAM switching	11 × 3 RRAM crossbar + CBRAM	Exp.	Possible	SNR controlled SA (Pulse width modulation)	Spin Glass	225 spins	All-to-all	Binary	N/A	Yes	N/A	N/A	N/A
IEDM 2019 [99]	RRAM	Intrinsic + External noise	64 × 64 crossbar	Exp.	Possible	SNR controlled SA (V_{READ} modulation)	Graph Partitioning	6 nodes	All-to-all	Analog	N/A	No	N/A	N/A	N/A
Nat. Electron. 2020 [62]	1T1R RRAM	Intrinsic noise	60 × 60 crossbar	Exp.	Possible	Noise-controlled SA (Hysteretic threshold modulation)	Max-Cut	60 nodes	All-to-all	Binary	N/A	No	72 nJ*	600 ns*	120.1 mW*
Sci. Adv. 2020 [104]	RRAM	N/A (Deterministic)	2 × 2 crossbar	Exp.	Possible	Transiently CSA (intrinsic LTD)	Max-Cut	2 nodes	All-to-all	Analog	N/A	No	N/A	N/A	N/A
IEDM 2021 [106]	1T1R RRAM	Random bias current	1152 × 1024 crossbar	Exp.	Possible	Random-bias-controlled SA	TSP	10 cities	All-to-all	5-level	N/A	Yes	N/A	N/A	44.76 mW
IEDM 2022 [98]	14-nm SONS FinFET	Intrinsic noise	FinFET crossbar	Device Exp. + System Sim.	Possible	SNR controlled SA (V_D modulation)	TSP	150 cities (Sim.)	All-to-all	5-bit	N/A	No	0.46 μJ**	2.78 ms**	0.165 mW**
Nat. Electron. 2024 [105]	1T1R RRAM	External digital randomness	128 × 128 crossbar + FPGA	Exp.	Possible	Simulated annealing	Max-cut / Graph coloring	1400 nodes	Sparse	Binary	N/A	Yes	N/A	N/A	N/A
Nano Energy 2025 [96]	RRAM	Intrinsic noise	32 × 32 crossbar	Exp.	Possible	SNR-controlled SA (V_{READ} modulation)	Max-Cut	32 nodes	All-to-all	Binary	10^3	No	3.35 pJ	N/A	N/A

N/A indicates that the corresponding metric was not reported in the original study or could not be directly extracted in a comparable form.

*System-level estimates based on experimentally grounded mem-HNN simulations scaled to a 16-nm technology node for 50 annealing cycles.

**System-level estimates based on measured device characteristics and a 14-nm FinFET circuit macro model including crossbar arrays and peripheral circuitry.

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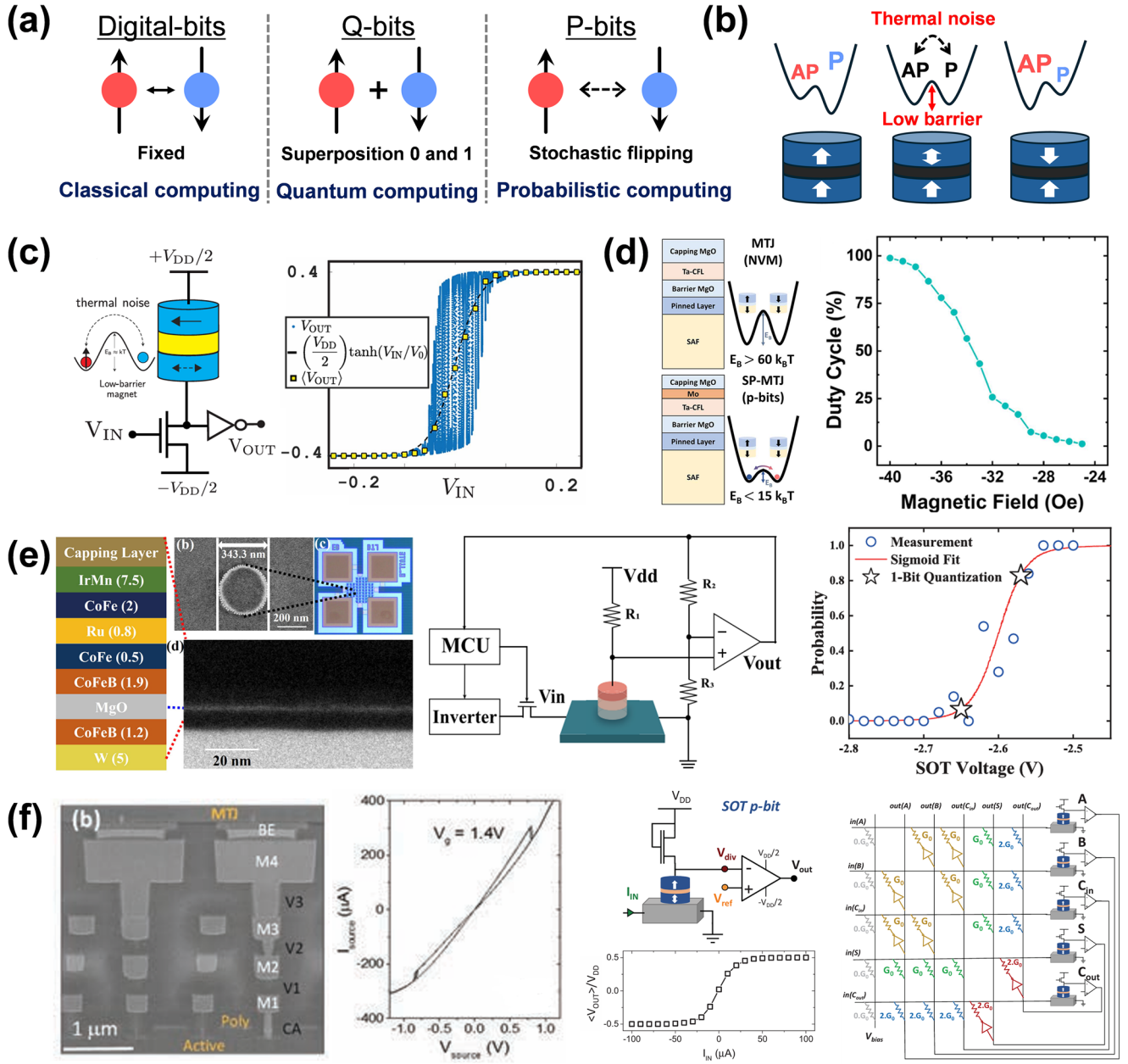

FIGURE 4 | Stochastic spin dynamics-based Ising machines. (a) Schematic comparison of digital bits, qubits, and p-bits. (b) Illustration of MTJ-based p-bit operation via thermally activated stochastic switching between parallel (P) and antiparallel (AP) states. (c) Embedded MRAM-based p-bit implemented by a compact modification of a 1T–1MTJ STT-MRAM cell, where the free layer is engineered as a low-barrier magnet enabling thermally driven stochastic switching (left panel), and p-bit characteristics showing instantaneous and time-averaged V_{OUT} as a function of V_{IN}, obtained from SPICE simulations, with the dashed line representing a tanh fit (right panel). Reproduced with permission [131]. Copyright 2020, IEEE. (d) Schematic of the stack configuration and comparison of energy barriers between MTJs with and without Mo insertion, where the additional Mo layer lowers the energy barrier and enables stochastic oscillation (left panel), and duty cycle as a function of external magnetic field for an SP-MTJ with 1.5 Å Mo insertion, exhibiting a Poisson-like distribution (right panel). Reproduced with permission [129]. Copyright 2026, IEEE. (e) Stack schematic of the MTJ layers and corresponding SEM, optical, and TEM images of the fabricated device (left panel), circuit diagram of the p-bit, in which each unit incorporates read and write circuits to process MCU control signals and generate the SOT voltage (middle panel), and measured switching probability of the SOT-based p-bit following an ideal sigmoid response (right panel). Reproduced with permission [135]. Copyright 2025, IEEE. (f) Cross-sectional SEM image of a 1T–1R MTJ and its switching characteristics (left panel), schematic of an SOT-biased p-bit and its SPICE-simulated input–output characteristics showing averaged output as a function of input current (middle panel), SOT-MTJ-based Ising network integrated with a memristor crossbar array (right panel). Reproduced with permission [136]. Copyright 2023, IEEE.

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thereby enhancing convergence in probabilistic computation. Using this SOT-MTJ p-bit array, the authors experimentally demonstrated the solution of combinatorial optimization problems, including XOR logic and integer factorization, achieving up to 90% accuracy with the proposed successive probability approach.

Recent approaches have explored crossbar array–based Ising architectures that utilize resistive networks to perform Hamiltonian computations, while incorporating MTJ-based p-bits to enable intrinsic stochastic behavior. In the context of SA, increasing the effective coupling strength or gain can be interpreted as a reduction in the effective temperature, gradually suppressing stochastic fluctuations and promoting convergence toward low-energy states [136–139]. Danouchi et al. demonstrated such a crossbar-based Ising computing architecture in 2023 using a resistive network to implement the Ising Hamiltonian, integrated with MTJ-based p-bits in a hybrid CMOS–MTJ system [136]. Figure 4f shows a cross-sectional SEM image of a 1T–1R MTJ along with its switching characteristics, and the SOT-based p-bit circuit, where decoupled read and write paths enable improved modulation of stochastic fluctuations and yield a well-defined sigmoidal response in the averaged output after digitization. The resistively coupled network architecture of SOT-MTJ p-bits is employed, in which weighted interactions are implemented through a resistor array to realize the Ising Hamiltonian. Using this architecture, the authors implemented Ising-based computational circuits, including a full-adder equivalent network and a larger-scale multiplier, demonstrating functionalities such as Boolean satisfiability solving and integer factorization through stochastic state evolution. This work demonstrates the feasibility of directly coupling stochastic p-bits through passive resistive networks for in-memory probabilistic computation. By reducing the data movement associated with externally computed interactions, this architecture suggests a potential route toward larger-scale stochastic Ising systems, although its scalability remains to be experimentally validated.

While MTJ-based p-bits represent one of the most mature and widely studied platforms for stochastic Ising machines, they still face challenges related to device variability, scalability, and precise control of low-barrier states despite their well-established fabrication processes and relatively controllable stochastic behavior. To overcome these limitations, alternative device technologies exhibiting intrinsic stochasticity, including diffusive memristors, NbO_x threshold switching elements, Cu-based conductive-bridge RAM (CBRAM), and perovskite nickelates, have been actively explored for p-bit implementation. These approaches utilize diverse physical mechanisms, such as filamentary dynamics, metal–insulator transitions, and ionic motion, to realize probabilistic switching behavior, enabling compact implementations without the need for complex magnetic structures. However, these devices often suffer from limited endurance, increased variability, and reduced controllability of stochastic characteristics. In parallel, significant efforts are being devoted to improving device endurance and reliability, which remain critical challenges for large-scale implementation [140–149]. As a result, each device platform presents distinct trade-offs between controllability, scalability, and energy efficiency, highlighting the importance of device-level optimization for the realization of practical stochastic Ising machines.

Park et al. demonstrated a p-bit based on hydrogen-doped perovskite nickelates in 2022, where stochastic resistance switching originates from the presence of multiple metastable hydrogen configurations within the lattice [149]. The device exhibits voltage-controlled probabilistic switching between high- and low-resistance states, resulting in a tunable sigmoidal activation function without relying on external random number generators. By utilizing these stochastic nickelate p-bits, the authors implemented a probabilistic computing architecture based on a shared-synapse crossbar network, enabling highly parallelized sampling. Using this framework, they successfully demonstrated the solution of combinatorial optimization problems, including integer factorization and Boolean satisfiability. Rhee et al. proposed a p-bit based on an NbO_x volatile memristor in 2023, in which probabilistic behavior arises from noise-induced metal–insulator transition dynamics [148]. By integrating the NbO_x device with a series resistor, a self-oscillatory circuit is formed, generating stochastic bitstreams without the need for external clocking signals. The oscillation probability can be continuously tuned by the applied voltage, exhibiting a sigmoidal relationship suitable for probabilistic computing. Using this NbO_x-based p-bit, the authors implemented a memristive Boltzmann machine and demonstrated its capability to solve combinatorial optimization problems, such as the minimum vertex cover problem, validating the feasibility of non-MTJ p-bit hardware for energy-based computing. These works highlight the potential of emerging material systems with intrinsic stochasticity as promising platforms for compact, energy-efficient, and highly parallel p-bit implementations, while also emphasizing the importance of balancing stochasticity, controllability, and device reliability for scalable hardware realization.

Representative p-bit implementations are quantitatively compared in terms of physical entropy source, sigmoid tunability, demonstrated scale, characteristic stochastic timescale, energy efficiency, and system-level performance, as summarized in Table 3. Magnetization-based p-bits, including STT-, SOT-, and SP-MTJs, offer low-energy stochastic switching and relatively mature device structures. Among the studies compared, STT-MTJ p-bits report switching energies as low as 2 fJ per bit, while SP-MTJ implementations have experimentally demonstrated networks of up to 80 p-bits [126, 135, 150]. However, their stochastic responses depend strongly on magnetic device parameters, and device-to-device variation can necessitate additional calibration or peripheral circuitry. In p-bit Ising machines, the local bias term acts as an external field that energetically favors one of the two spin states depending on its sign and magnitude. In the SMTJ-based implementation, the bias contribution is incorporated into the input current together with the weighted interaction terms, with the resulting analog input generated using DAC-controlled peripheral circuitry [150]. Therefore, programmable local-bias implementation requires additional signal-generation, control, and routing resources, which can contribute to peripheral-circuit overhead as the network scales. Volatile and diffusive memristor p-bits provide stochastic dynamics arising from metal–insulator transitions or volatile threshold switching, while nickelate devices exploit proton migration to generate probabilistic responses [144, 148, 149]. NbO_x and nickelate implementations further demonstrate electrical tunability of their probabilistic characteristics. Nevertheless, most of these non-MTJ approaches have so far been experimentally validated at

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TABLE 3 | Quantitative comparison of representative p-bit hardware platforms in terms of hardware implementation, physical entropy source, sigmoid tunability, demonstrated scale, characteristic stochastic timescale, energy, and computational performance.

Reference	Representation of spins	Physical entropy source	Demo complexity	Exp./ Sim.	Tunability of Sigmoid response	CMOS compatibility	Problem type	Problem scale	Connectivity	Stochastic time constant	Endurance	Energy per bit	Energy to solution	Time to solution	Power
Nature 2019 [126]	STT-MTJ	Magnetization	8 STT p-bits + MCU/DAC	Exp.	N/A	Possible	Integer factorization	8	All-to-all	100 ps	N/A	2 fJ	N/A	N/A	N/A
IEEE Trans. Electron Devices 2025 [135]	SOT-MTJ	Magnetization	8×2 SOT p-bit array	Exp.	N/A	Possible	Integer factorization	16	All-to-all	4.56 µs	N/A	N/A	N/A	N/A	N/A
Nat. Commun. 2024 [150]	SMTJ	Magnetization	80 SMTJs + PCB system	Exp.	N/A	Possible	Traveling salesman problem	70	All-to-all	123 µs	N/A	N/A	2.56×10^{-2} J	40 s	640 µW
Nat. Commun. 2023 [148]	Volatile memristor	Metal-insulator transition	Single	Device Exp. + System Sim.	Tunable	Possible	Minimum vertex covering	6 (Sim.)	All-to-all	260 ns	N/A	128 pJ	N/A	N/A	N/A
Nat. Commun. 2022 [144]	Diffusive memristor	Volatile threshold switching	3 memristor + FPGA	Exp.	N/A	Possible	Integer factorization	8 (Sim.)	All-to-all	85 ps	$>10^6$	N/A	N/A	N/A	154 nW
Nano Lett. 2022 [149]	Nickelate	Proton migration	Single	Device Exp. + System Sim	Tunable	Hard	Integer factorization	12 544 (Sim.)	All-to-all	>9 ns	N/A	< 0.1 pJ	N/A	N/A	N/A
Adv. Funct. Mater. 2024 [151]	n-p-n biristor	Single transistor latch	Single	Device Exp. + System Sim	N/A	Possible	Logic, max-SAT	4 (Sim.)	All-to-all	< 30 ns	$>10^{13}$	N/A	N/A	N/A	582 nW

N/A indicates that the corresponding metric was not reported in the original study or could not be directly extracted in a comparable form.

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the individual-device or small-device-count level, with larger optimization tasks evaluated through simulations based on measured device characteristics rather than fully integrated p-bit networks. The n-p-n biristor provides a semiconductor-based stochastic implementation with potential CMOS compatibility, although its reported optimization task was likewise evaluated using a fitted device response rather than a fully integrated p-bit network [151]. Taken together, these comparisons indicate that device-level stochasticity alone does not determine system-level scalability. The achievable network scale also depends critically on the integration of weighted coupling, probability-control circuitry, and peripheral interfaces. Future p-bit hardware therefore requires tighter on-chip integration of stochastic devices and coupling networks, together with controllable probabilistic responses, to translate device-level advantages into larger-scale system implementations.

3.3 | Oscillator-Based Ising Machines

In oscillator-based Ising machines (OIMs), the phase dynamics of coupled oscillators are exploited to encode and solve combinatorial optimization problems. In this framework, each oscillator represents a spin variable, and its phase state, typically encoded as 0° and 180°, corresponds to binary spin values of +1 and −1, respectively. The interactions between spins are mapped onto the coupling between oscillators, such that in-phase and anti-phase locking behaviors emulate ferromagnetic and antiferromagnetic interactions in the Ising model. As illustrated in Figure 5a, an Ising graph corresponding to a given optimization problem can be directly translated into a network of coupled oscillators. When the oscillator network operates under SHIL, a bistable phase landscape is induced, enabling each oscillator to stabilize at one of two phase states. The collective dynamics of the network evolve as a continuous-time nonlinear system, where phase synchronization and competition among oscillators naturally drive the system toward configurations that minimize an effective energy function analogous to the Ising Hamiltonian. This continuous-time evolution enables implicit energy minimization without discrete state updates, distinguishing OIMs from conventional annealing-based approaches.

In addition to deterministic phase locking, noise plays a crucial role in OIMs. Phase noise, originating from device-level fluctuations and circuit-level perturbations, introduces stochasticity into the phase dynamics, enabling the system to escape metastable states and explore the energy landscape more effectively. This stochastic behavior is analogous to thermal fluctuations in simulated annealing and can significantly enhance the probability of reaching near-optimal solutions. However, excessive phase noise may disrupt stable phase synchronization and degrade solution accuracy. Therefore, careful control of phase noise is essential to balance exploration and convergence, highlighting a trade-off between stochastic search capability and synchronization stability in oscillator-based Ising systems. This trade-off is a fundamental factor that determines both solution quality and scalability in large oscillator networks.

Insulator-to-metal transition materials, particularly VO_2, have attracted significant attention as promising candidates for compact oscillator-based Ising machines due to their abrupt conductivity switching and intrinsic hysteretic dynamics [152–156]. Figure 5b shows a VO_2-based device, where the insulator-to-metal phase transition enables nonlinear switching characteristics suitable for realizing relaxation oscillators, and the oscillator-based mapping of the max-cut problem [157]. Each node in the input graph is represented by a VO_2 oscillator, while edges are translated into coupling elements that define the interaction strength between oscillators. The problem is formulated based on the Ising Hamiltonian, where each oscillator corresponds to a spin variable $s_i \in [+1,-1]$, encoded by its phase. The coupling coefficients J_{ij} are implemented through capacitive interconnections, enforcing phase relationships between oscillators. The objective of max-cut is to partition the graph into two groups such that the total weight of the edges crossing the partition is maximized, which is achieved by driving coupled oscillators toward anti-phase synchronization. However, due to multi-body interactions in densely connected networks, the system may not naturally converge to strictly binary phase states. To address this, a SHIL signal is introduced. By injecting a signal at twice the natural oscillation frequency ($f_{SHIL} = 2f_{osc}$), the phase space is quantized into two stable states separated by π, ensuring robust phase binarization. Under these conditions, the coupled oscillator network performs analog energy minimization, where the system dynamics evolve toward the ground state of the Ising Hamiltonian. The right panel of Figure 5b presents the max-cut solution and the corresponding phase relationships of the coupled VO_2 oscillators under SHIL. The oscillators are clearly partitioned into two distinct phase groups, one near 0° (in-phase) and the other near 180° (out-of-phase) with respect to a reference oscillator. This binary phase separation directly encodes the spin states, and nodes belonging to different partitions exhibit anti-phase relationships, thereby maximizing the cut edges [158–162]. Experimentally, however, the two SHIL-stabilized phase states can exhibit finite phase dispersion, with stronger injection producing tighter phase confinement around the two binary states. These results demonstrate that SHIL-enabled phase quantization is critical for ensuring robust binary encoding and stable convergence in oscillator-based Ising machines. For Ising formulations containing local bias terms, an additional injection signal at the fundamental oscillation frequency f_{osc} can be used to implement the external bias. In the Max-3SAT implementation, this bias signal was applied together with a second-harmonic signal at $2f_{osc}$, where the former provides the local bias and the latter enables phase binarization through SHIL [157]. The generation and distribution of the bias injection signal therefore introduce additional circuit and control overhead in practical OIM implementations.

In addition, biristor-based oscillators have recently emerged as a promising alternative for implementing large-scale oscillator-based Ising machines [163–169]. Figure 5c shows a vertically integrated InGaAs biristor device fabricated in a BEOL-compatible structure [167]. The biristor exhibits a characteristic S-shaped current–voltage behavior with a well-defined hysteresis window, as shown in the second panel, which is essential for generating self-sustained oscillations. The oscillatory behavior of the biristor originates from impact ionization–induced positive feedback. When the applied voltage exceeds a threshold (V_{LU}), a strong electric field is established across the InGaAs channel, triggering impact ionization and generating electron–hole pairs. The generated carriers further increase the electric field through internal feedback, leading to a sudden transition from a high-

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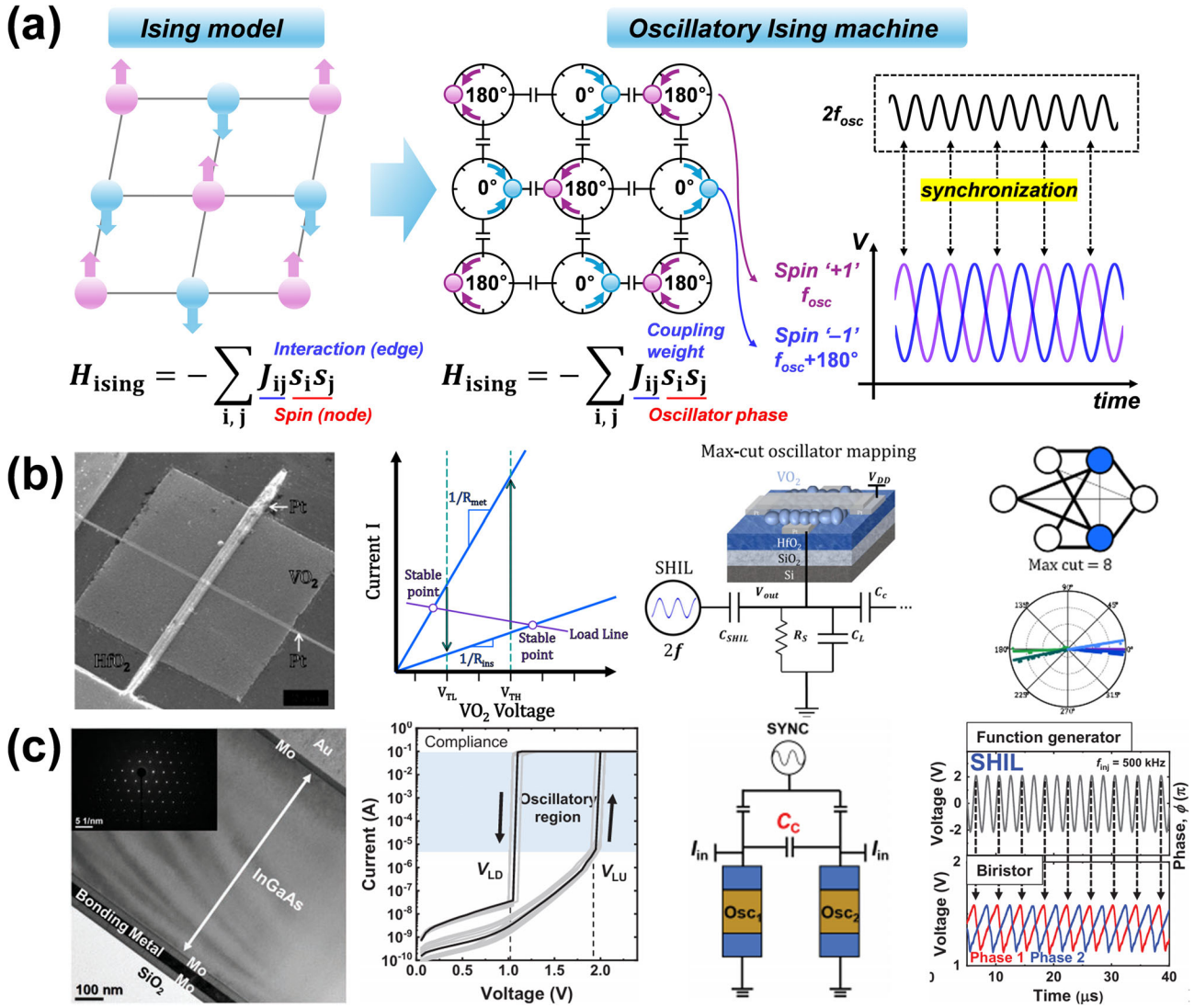

FIGURE 5 | Coupled oscillator-based Ising machines. (a) Conceptual schematic of an oscillatory Ising machine, where spin states are encoded by the phase of oscillators. Under an external injection signal at twice the natural frequency (2*f*), the oscillators exhibit injection locking and synchronize either in-phase (0°) or out-of-phase (180°), corresponding to spin states of +1 and −1, respectively. (b) VO_2-based relaxation oscillator. The left panel shows an SEM image of the VO_2 device. The middle panel illustrates the threshold switching behavior of VO_2, where the device transitions to a metallic state when the applied voltage exceeds the threshold voltage (V_{TH}), and returns to the insulating state when the voltage falls below the holding voltage (V_{TL}), resulting in self-sustained oscillations. The right panel shows a coupled oscillator network, where interactions between spins are implemented via capacitive coupling. Under external injection at twice the oscillation frequency, the oscillators synchronize into distinct phase states. Reproduced with permission [157]. Copyright 2024, Springer Nature. (c) Cross-sectional TEM image showing a Mo/InGaAs/Mo biristor used for spin representation (left panel). The middle panel illustrates the oscillation mechanism driven by impact ionization, where charge accumulation lowers the potential barrier and increases conduction until a threshold is reached, followed by rapid discharge that restores the high-resistance state, resulting in self-sustained oscillations. The coupling strength between spins is controlled by a coupling capacitor (C_c), enabling phase synchronization into distinct phase states. Reproduced with permission [167]. Copyright 2023, IEEE.

resistance state to a low-resistance state (latch-up). Subsequently, as the voltage drops below a lower threshold (V_{LD}), the impact ionization process is suppressed, and the device returns to the high-resistance state. This repetitive latch-up and release mechanism enables relaxation oscillation when the device is combined with external passive components [165, 166]. Such oscillators can be capacitively coupled, where the coupling capacitor C_c defines the interaction strength between oscillators. The synchronization behavior of coupled biristor oscillators is determined by their nonlinear dynamics and coupling conditions, enabling phase-based information encoding similar to other oscillator-based Ising systems. The right panel of Figure 5c shows the measured oscillation waveforms under subharmonic injection locking SHIL. The oscillation frequency of the biristor-based oscillator depends on the charging and discharging dynamics of the parasitic capacitance and can be expressed as:

$$f_{osc} = \frac{I_{in}}{C_{par}(V_{LU} - V_{LD})}. \quad (5)$$

Here, I_{in} is the input current, C_{par} is the effective parasitic capacitance, and V_{LU} and V_{LD} denote the upper and lower threshold

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voltages associated with the latch-up and release transitions, respectively. This relation indicates that the oscillation frequency can be tuned by controlling the input current and intrinsic device parameters. When multiple oscillators are coupled through a capacitance C_c, the interaction between oscillators modifies their charging dynamics, thereby influencing both the oscillation frequency and phase relationship. By injecting a periodic SHIL signal, the oscillator phases are stabilized into discrete phase states, as indicated by the two phase trajectories (Phase 1 and Phase 2). This phase locking behavior demonstrates that biristor-based oscillators can provide compact, CMOS-compatible building blocks for scalable oscillator-based Ising machines. Spintronic nano-oscillators, including spin-torque nano-oscillators (STNOs) and spin-Hall nano-oscillators (SHNOs), have also been explored for oscillator-based Ising machines [170–173]. Their GHz-range magnetization dynamics and nanoscale footprint offer the potential for high-speed and compact Ising computation, while second-harmonic injection locking can stabilize two phase states separated by π for binary spin representation. Numerical and experimental studies have demonstrated Max-Cut solving using STNO and SHNO networks, ranging from hundreds of simulated STNOs to small experimental SHNO arrays [170, 172]. More recent studies have further explored programmable and adaptive spintronic oscillator platforms, although scalability remains constrained by oscillator coupling, synchronization, and network-level interconnection complexity [171, 173].

The quantitative characteristics and trade-offs of representative OIM implementations are compared in terms of interaction scheme, demonstrated scale, connectivity, operating frequency, and system-level performance, as summarized in Table 4. CMOS ring-oscillator OIMs have achieved the largest experimental scale, reaching 1,968 oscillators, although this implementation employs a sparse topology with up to eight neighboring connections per oscillator [174]. In contrast, a fully connected N-oscillator network requires $N(N-1)/2$ pairwise coupling links, causing the coupling hardware to grow quadratically with system size. Fully connected CMOS implementations have so far been demonstrated with 59 oscillators [175], while emerging-device OIMs based on VO_2, InGaAs biristors, and spin Hall nano-oscillators have mainly been demonstrated at smaller scales [157, 165, 166, 170, 176, 177]. Across these platforms, coupling is physically implemented through capacitive, resistive, logic-based, or magnetodipolar interactions, making dense and independently programmable connectivity increasingly demanding as the oscillator count increases. Interconnect loading and parasitic capacitance can further modify the oscillator and coupling dynamics, while device-to-device variation produces frequency dispersion that can reduce the synchronization margin. Competing interactions among multiple coupled oscillators can give rise to phase frustration, in which the preferred pairwise phase relationships cannot be simultaneously satisfied. The severity of such phase frustration depends on the network topology and coupling configuration, thereby affecting convergence behavior and practical solution quality and potentially limiting system scalability.

The robustness of phase binarization also depends on the injection-locking conditions. In SHIL-based OIMs, insufficient injection strength can result in broader phase distributions and weaker confinement around the desired $0/\pi$ states, whereas stronger injection improves phase locking at the cost of additional driving requirements. Consequently, coupling strength and injection conditions must be designed together with the intrinsic frequency dispersion and phase noise of the oscillator network. System-level implementation also requires phase readout, control, and, depending on the architecture, programmable coupling circuitry, whose area, energy, and communication overhead can become significant as the network scales. Overall, the scalability of OIMs is therefore determined not only by the intrinsic oscillator dynamics but also by synchronization robustness, phase stability, coupling programmability, and the ability to realize dense coupling and readout networks with manageable hardware overhead.

4 | Key Issues and Design Challenges in Emerging Device-Based Ising Machines

One of the key challenges in emerging- device-based Ising machines is the sparsity of the interaction adjacency matrix, which directly impacts hardware utilization efficiency and scalability in crossbar-based implementations. In such architectures, the interaction matrix is directly mapped onto the array to perform matrix–vector multiplication for evaluating the Ising energy [62]. However, when the connectivity of the target combinatorial optimization problem is sparse, a significant portion of the crossbar array remains unused, leading to inefficient resource utilization and increased memory overhead [178–182]. This issue can be addressed through matrix remapping techniques. Figure 6a illustrates a schematic of such a remapping approach, which reduces the impact of sparsity by restructuring the interaction matrix. A systematic matrix compression procedure reduces the effective size of the interaction matrix by eliminating redundant rows and columns [178]. The process consists of four sequential steps. First, the nodes are sorted in ascending order of their degree $D(x_i)$, prioritizing the pruning of sparsely connected nodes. This ordering enables rows and columns associated with weakly connected variables to be processed first, facilitating subsequent compression. Next, row and column compression are performed by exploiting the symmetry of the QUBO (quadratic unconstrained binary optimization) matrix $Q = Q^T$. For a compressible row or column, its non-zero off-diagonal elements are accumulated into the corresponding diagonal entries, effectively transferring interaction contributions while preserving the quadratic form $x^T Qx$. Once these contributions are relocated, the corresponding row or column can be entirely zeroed out, thereby eliminating unnecessary hardware allocation without altering the problem formulation. Finally, the compressed matrix Q' is mapped onto the crossbar array through a variable partitioning scheme, where the original variable vector is decomposed into two asymmetric input vectors applied along rows and columns. This transformation preserves the original energy function while enabling significantly more compact hardware mapping. As a result, redundant rows and columns are removed, leading to a significant reduction in hardware resources. This approach can reduce the required chip area by up to 75%. However, this approach introduces a trade-off in the form of preprocessing overhead. Node reordering, identification of compressible rows and columns, and variable partitioning must be performed prior to mapping the problem onto the crossbar, typically on external control hardware such as a host CPU or FPGA.

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TABLE 4 | Comparison of representative oscillator-based Ising machines in terms of oscillator implementation, spin representation, demonstrated scale, interaction scheme, connectivity, operating frequency, and reported energy, time, and power characteristics.

Reference	Representation of spins	Interaction	Demo complexity	Exp./ Sim.	CMOS compatibility	Problem type	Problem size	Connectivity	Operation frequency	Endurance	Energy to solution	Time to solution	Power
Nat. Electron. 2022 [174]	Ring oscillator	Transmission gate	CMOS Ising chip	Exp.	Possible	Random Ising graph	1968	Sparse	1 GHz	N/A	N/A	50 ns	42 mW
Nat. Electron. 2025 [175]	Ring oscillator	CMOS inverter	CMOS Ising chip	Exp.	Possible	QUBO	59	All-to-all	5.36 MHz	N/A	N/A	N/A	10 mW
IEDM 2019 [176]	VO_2 oscillator	Capacitive coupling	4-PTNO network	Exp.	Hard	Max-cut	4	All-to-all	100 kHz	N/A	N/A	N/A	N/A
Nat. Electron. 2022 [177]	VO_2 oscillator	Capacitive coupling	8-PTNO network	Exp.	Hard	Max-cut	8	All-to-all	60-70 kHz*	N/A	76.8 nJ*	30 µs*	2.56 mW*
Nat. Commun. 2024 [157]	VO_2 oscillator	Capacitive coupling	9-VO_2 network	Exp.	Possible	Graph coloring Max-cut / Max-3SAT	9	Sparse	~2 kHz	N/A	N/A	11.5 ms	180 µW
Small 2024 [166]	InGaAs biristor	Capacitive coupling	4-biristor network	Exp.	Possible	Max-cut	4	All-to-all	250 kHz	N/A	120 nJ*	3 µs*	N/A
Adv. Sci. 2025 [165]	InGaAs biristor	FeFET switch	4-biristors + 6-FeFETs network	Exp.	Possible	Max-cut	4	Sparse	250 kHz	$>10^9$	5.5 nJ**	1.11 µs	N/A
Phys. Rev. Applied 2022 [170]	SHNO	Magnetodipolar coupling	2×2 SHNO array	Exp.	Possible	Max-cut	4	All-to-all	7.8 GHz	N/A	4 mJ***	21 µs***	180 W***
Appl. Phys. Lett. 2021 [172]	STNO	Oscillator coupling	288-STNO network	Sim.	Possible	Max-cut	288	Sparse	~ 3.2 GHz	N/A	N/A	~ 100 ns	N/A

N/A indicates that the corresponding metric was not reported in the original study or could not be directly extracted in a comparable form.

*Projected for a 100-node, 50%-density Max-cut problem using the oscillation frequency expected from device-size scaling.

**Calculated using a projected oscillation frequency with size scaling.

***System-level estimates based on 2 × 2 SHNO array for a 5000-SHNO syste

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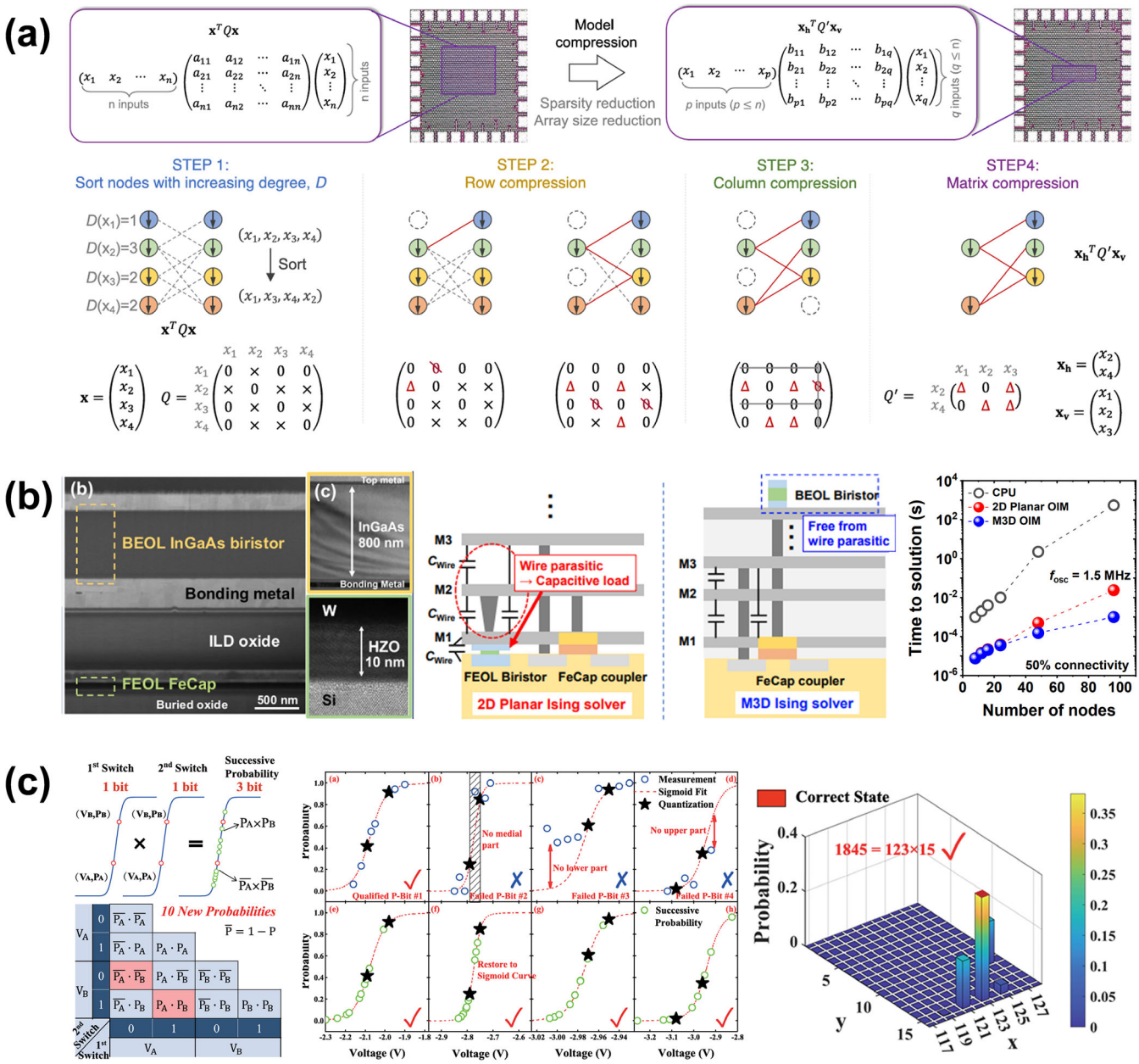

FIGURE 6 | Key challenges and architectural solutions in emerging-device-based Ising machines. (a) Matrix remapping and compression technique for addressing sparsity in crossbar-based Ising machines. The interaction matrix Q is reordered based on node degree, followed by row and column compression exploiting the symmetry $Q = Q^T$, where off-diagonal elements are relocated to diagonal entries, enabling redundant rows and columns to be eliminated. The compressed matrix Q' is then mapped onto a reduced crossbar using a variable partitioning scheme, preserving the original energy function while significantly reducing array size. Reproduced with permission [178]. Copyright 2024, Springer Nature. (b) Delay issue and mitigation in oscillator-based Ising machines. The left panel shows a cross-sectional TEM image of the monolithic 3D architecture integrating an InGaAs-based biristor (oscillator) and a FEOL ferroelectric capacitor (FeCAP, HZO ~10 nm) for coupling. In conventional 2D planar implementations, long interconnects introduce significant parasitic capacitance, leading to increased propagation delay and reduced oscillation frequency. The proposed 3D integration shortens the coupling path and minimizes parasitic loading, thereby suppressing phase distortion and frequency degradation. Reproduced with permission [164]. Copyright 2025, IEEE. (c) Peripheral-circuit overhead reduction in stochastic p-bit Ising machines. The left panel illustrates the successive probability approach, in which two consecutive stochastic switching operations generate more than 3-bit probability resolution within a 1-bit quantization framework. The middle panel presents measured sigmoid probability characteristics of four representative SOT p-bit devices and their reconstructed probability responses, demonstrating improved tolerance to nonideal device characteristics. The right panel shows successful factorization of the integer 1845 with an accuracy of 38.2% using the successive probability approach while maintaining the simplified 1-bit hardware framework. Reproduced with permission [135]. Copyright 2025, IEEE.

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Another critical challenge in emerging-device-based Ising machines arises in oscillator-based dynamical systems, where delay plays a fundamental role in determining system performance. In oscillator-based Ising machines, the coupling between spins is realized through phase interactions among oscillators, and the system evolves toward a minimum-energy configuration via synchronization dynamics. However, in practical hardware implementations, signal propagation delays introduced by interconnects and coupling elements can significantly degrade both convergence speed and solution quality [183–185]. These delays originate from parasitic capacitance and resistance in the interconnect network, as well as device-level coupling elements. In conventional planar implementations, long wire lengths between oscillators lead to substantial capacitive loading, which slows down signal propagation and introduces phase lag in the coupling network. More importantly, the increased parasitic capacitance $C_{\text{parasitic}}$ can directly raise the effective load of the oscillator circuit, significantly reducing the oscillation frequency f_{osc}. This reduction in operating frequency slows down the intrinsic dynamics of the system, thereby increasing the time required for phase evolution and synchronization. As a result, physical interconnect distance becomes a critical factor linking circuit-level delay to system-level optimization performance.

This phase lag effectively distorts the intended interaction between spins, resulting in a mismatch between the designed coupling strength and the effective phase interaction. Consequently, the system may converge to incorrect or suboptimal states, and the time required to reach a stable solution increases rapidly with system size, limiting scalability. Figure 6b shows a cross-sectional TEM image of the proposed monolithic 3D oscillator-based Ising machine [164]. The structure integrates an InGaAs-based biristor in the BEOL as the oscillatory element representing spins, while the coupling between spins is implemented using a ferroelectric capacitor located in the FEOL. The ferroelectric capacitor is based on a thin HZO layer (~10 nm), enabling compact and energy-efficient capacitive coupling with multi-weight programmability. By vertically integrating the coupling element directly beneath the oscillator, the physical distance between interacting nodes is significantly reduced compared to conventional planar layouts. This vertical integration fundamentally alters the delay characteristics of the system. In the 2D planar architecture, coupling signals must propagate through long lateral interconnects, introducing large parasitic capacitances and associated RC delays. In contrast, the monolithic 3D structure minimizes lateral wiring and replaces it with short vertical interconnect paths, effectively reducing the capacitive load and signal propagation delay [186, 187]. As a result, delay-induced phase lag is substantially suppressed, and the oscillation frequency degradation is mitigated, allowing the oscillator network to operate at higher speeds while maintaining accurate phase relationships during synchronization. The impact of this reduction in physical distance is reflected in the right panel of Figure 6b, where the time-to-solution is significantly improved compared to conventional 2D planar and CPU-based implementations. The reduced delay enables faster phase synchronization across the network, leading to accelerated convergence toward the minimum-energy state. Therefore, delay is not merely a circuit-level artifact but a critical system-level factor that directly impacts the dynamics of oscillator-based Ising machines. Effective mitigation of delay through architecture–device co-design, such as monolithic 3D integration, is essential for achieving scalable, high-speed, and energy-efficient Ising machine hardware.

Another important challenge in emerging-device-based Ising machines is the peripheral-circuit overhead required for accurate probability generation. This issue is particularly relevant to stochastic p-bit Ising machines, where representing a wide range of coupling strengths requires sufficiently fine probability resolution. Conventional implementations may therefore rely on high-resolution DACs and well-calibrated sigmoid characteristics, increasing peripheral-circuit area and power while imposing stringent requirements on device uniformity. To address this limitation, Zhang et al. proposed a successive probability approach that maintains a 1-bit quantization framework while achieving multibit probability resolution through temporal probability composition rather than additional voltage levels [135]. As shown in Figure 6c, two consecutive stochastic switching events are combined to generate multibit probability resolution, allowing the writing circuit to be implemented using a simple 1-bit DAC such as an inverter or buffer. The middle panel shows that the reconstructed probability responses recover near-ideal sigmoid characteristics even from nonideal SOT p-bit devices, indicating improved tolerance to D2D variation and nonideal switching characteristics. The right panel further demonstrates successful factorization of the integer 1845 with an accuracy of 38.2%, whereas the conventional 1-bit quantization scheme fails to correctly solve the same problem. Despite these advantages, temporal probability composition introduces additional trade-offs. Generating finer probability resolution requires repeated stochastic switching and additional sampling events, which increase the number of device operations and computational latency and may impose more stringent endurance requirements. Therefore, reducing peripheral-circuit complexity cannot be considered independently of probability resolution, device variation, reliability, and computational latency, and these factors should be co-optimized for scalable stochastic Ising-machine hardware.

Beyond the challenges discussed above, several additional issues should be considered for the practical realization of large-scale Ising hardware. At the device level, device-to-device and cycle-to-cycle variation, temporal drift, endurance limitations, and nonideal stochastic or dynamical characteristics can degrade the stability, reproducibility, and long-term reliability of computation. The relative importance of these nonidealities depends strongly on the device platform and the physical mechanisms used for spin representation and interaction. At the circuit and architecture levels, practical implementations face additional challenges associated with signal sensing and conversion, peripheral-circuit complexity, limited weight and signal precision, representation of signed interactions, array and coupling-network scalability, and hardware-efficient implementation of annealing or stochastic-control schemes. These factors directly influence computational accuracy, energy efficiency, latency, and hardware utilization. From a system perspective, efficient problem mapping, optimization strategies, and standardized evaluation methodologies are equally important for meaningful comparison across different hardware platforms. In particular, benchmarking should distinguish experimentally demonstrated hardware performance from simulated or projected results and compare equivalent

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problem instances using common metrics such as solution quality, success probability, time-to-solution, energy-to-solution, and effective problem scale. Comparisons with optimized classical heuristics are also necessary to determine whether improvements at the device or circuit level translate into meaningful end-to-end computational advantages. System-level evaluation should include peripheral circuits, coupling networks, data movement, control, and mapping overhead, since improvements in intrinsic device characteristics do not necessarily translate directly into end-to-end performance gains. Therefore, future development of emerging-device-based Ising machines should pursue the co-optimization of devices, circuits, architectures, and algorithms to achieve scalable, reliable, and energy-efficient Ising computing systems.

5 | Conclusion and Prospects

Despite the broad range of applications explored using emerging-device-based Ising machines, most demonstrations have so far been performed on relatively small problem instances or with limited experimentally integrated hardware. Advancing these approaches toward practical large-scale systems will therefore require simultaneous improvements in scalability, connectivity, energy efficiency, operating speed, and hardware reliability. Importantly, the dominant bottleneck differs across device platforms, indicating that future progress will require platform-specific device–architecture–algorithm co-design rather than improvements at the device level alone. No single emerging device platform is likely to provide a universal solution across all Ising-machine architectures because each computational paradigm exploits a different physical primitive. Crossbar-based devices are particularly attractive for dense interaction storage and analog weighted accumulation, stochastic devices provide a natural route to hardware-native probabilistic spin updates, and oscillator-based devices offer intrinsically parallel phase dynamics. Therefore, the most promising device technology depends on whether its intrinsic physical advantages can be preserved after incorporating the coupling networks, peripheral circuits, and control hardware required for system-level operation.

For crossbar-based Ising machines, scaling to larger optimization problems requires careful consideration of array-level nonidealities. The number of problem nodes is directly mapped to the physical array dimension, whereas larger arrays increasingly suffer from IR drop, sneak-path currents, device variation, and yield degradation. Future systems may therefore benefit from architectural approaches that partition large problems across multiple smaller arrays, such as multi-tile architectures, together with algorithmic techniques that exploit sparsity or structured coupling to compress large interaction matrices into smaller hardware resources. Such approaches can reduce the physical array size required for a given problem while mitigating the nonidealities associated with monolithic scaling, although partitioning also introduces inter-array communication, routing, and accumulation overhead. Accordingly, a meaningful next scaling milestone for crossbar-based systems is not simply a larger monolithic array, but experimentally validated multi-array operation in which array nonidealities, inter-array communication, and peripheral overhead are explicitly included in system-level evaluation.

For p-bit-based Ising machines, a major gap remains between device-level stochastic demonstrations and larger experimentally integrated networks. Most non-MTJ p-bit studies have evaluated optimization performance through simulations based on measured device characteristics, whereas large-scale physical p-bit networks remain limited. Because probabilistic computation is sensitive to device-to-device and cycle-to-cycle variation, larger hardware demonstrations are required to verify whether stochastic responses remain sufficiently uniform and controllable as the network scale increases. The implementation of weighted interactions is another critical issue. Although intrinsic stochastic switching can reduce the need for externally generated randomness, DACs, control circuits, and coupling networks can dominate system-level area and power consumption. In addition, p-bit implementations relying on repeated physical switching should consider endurance as a system-level constraint for long-running sampling and optimization tasks. Future scaling should therefore move beyond isolated stochastic-device demonstrations toward experimentally integrated multi-p-bit networks with programmable weighted interactions, while verifying that device-level advantages in stochasticity and energy are retained after including coupling and peripheral circuitry.

For oscillator-based Ising machines, CMOS ring-oscillator implementations have demonstrated relatively large networks, whereas emerging-device oscillators such as VO_2, biristor, STNO, and SHNO platforms remain at smaller experimental scales. Their principal advantage is that Ising interactions can be represented directly through oscillator synchronization and phase dynamics, reducing the need for explicit digital evaluation of the Hamiltonian. However, programmable coupling becomes increasingly difficult as the network size grows. In particular, a fully connected network of N oscillators requires $N(N-1)/2$ pairwise coupling links, leading to rapidly increasing interconnect complexity, parasitic loading, and synchronization sensitivity. Frequency dispersion, phase noise, and device variation can further reduce synchronization robustness as the network scales. Consequently, a critical scaling milestone for OIMs is the experimental realization of larger networks with programmable long-range coupling while maintaining robust phase synchronization and preserving the intrinsic speed and parallelism of oscillator dynamics. These considerations indicate that, across all three emerging-device platforms, realistic scaling targets should be defined not solely by nominal spin or device count but by the scale at which the relevant computational primitive, connectivity, and system-level performance are experimentally maintained.

More importantly, claims of practical advantage should be supported by experimentally integrated system-level demonstrations rather than device-level metrics or projected scaling alone. Such validation should include direct benchmarking against optimized classical algorithms or established Ising solvers on comparable problem instances using experimentally measured solution quality, success probability, time-to-solution, and energy-to-solution. Benchmarking should clearly distinguish experimentally measured results from simulated or projected performance and account for peripheral circuits, coupling networks, data movement, control, and problem-mapping overhead. Comparisons should also employ equivalent problem definitions, solution-quality criteria, and stopping or success conditions to avoid apparent performance advantages arising

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from inconsistent benchmarking methodologies. Demonstrating that improvements persist as both the problem size and experimentally integrated hardware scale increase will be essential for establishing practical competitiveness. Despite these challenges, emerging-device-based Ising machines remain promising because they can directly exploit device conductance, stochastic switching, and oscillator dynamics as computational resources. Such physical implementations offer opportunities to reduce specific hardware and energy overheads while enabling compact and highly parallel optimization systems. Realizing this potential will require continued device-to-system co-design to ensure that advantages originating from intrinsic device physics are preserved through circuit, architecture, and system-level implementation.

Author Contributions

Sangwook Youn: conceptualization, Writing – original draft, visualization. **Hwiho Hwang**: conceptualization, writing – original draft, formal analysis. **Jaeung Lee**: methodology, investigation. **Heesu Seo**: methodology, investigation. **Hyungjin Kim**: writing – review and editing, supervision.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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