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RESEARCH ARTICLE

An 8-GS/s 7-bit Eight-Way Time-Interleaved Partially Speculative Loop-Unrolled SAR ADC

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ABSTRACT This paper presents an 8-GS/s, 7-bit, eight-way time-interleaved partially speculative loop-unrolled (PSLU) successive approximation register (SAR) analog-to-digital converter (ADC). The proposed speculative method improves conversion speed by immediately converting two capacitive digital-to-analog converter (CDAC) outputs after the comparator's aperture window, reducing the conversion cycle to the sum of the aperture window, logic delay, and CDAC settling time. To improve efficiency, the speculative conversion is applied only to the upper-bit decisions, providing an optimal trade-off between speed and power consumption. In addition, a time-domain conversion (TDC) scheme resolves the least significant bit without requiring an extra conversion cycle, avoiding hardware overhead. To achieve the required bandwidth while ensuring high accuracy, the proposed PSLU SAR ADC is time-interleaved in a direct sampling architecture with a transmission-gate-based clock distribution circuit. Fabricated in a 28-nm CMOS process, the eight-way time-interleaved 7-bit prototype achieves an 8-GS/s sampling rate, with a signal-to-noise-and-distortion ratio (SNDR) of 34.6 dB, a spurious-free dynamic range (SFDR) of 51 dB, and a power consumption is 19.7 mW. The Walden and Schreier figure-of-merit (FoM_W and FoM_S) are 56.1 fJ/conversion-step and 147.7 dB, respectively.

INDEX TERMS Analog-to-digital converter (ADC), partial speculative conversion, successive approximation register (SAR), time-domain conversion (TDC), time-interleaving.

I. INTRODUCTION

High-speed wireline communication systems increasingly demand analog-to-digital converters (ADCs) with sampling rates exceeding several tens of gigasamples per second and resolutions of 6–8 bits. Achieving such high sampling rates typically requires time-interleaved multi-channel ADCs [2], [3], [4], [5], [6]. As the target sampling rate increases, higher interleaving factors enable the use of moderate-speed

sub-ADCs in multi-channel architectures. However, a higher interleaving factor increases the input loading on the preceding interleaver due to routing parasitic, reducing overall power efficiency. Consequently, an ADC operating above 1 GS/s per channel is essential, as it lowers the required interleaving factor for a given overall sampling rate, increasing the achievable bandwidth and simplifying multi-channel ADC design.

According to the ADC performance survey, successive-approximation-register (SAR) ADCs with sampling rates above 100 MHz are widely adopted due to their

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architectural simplicity and power efficiency, accounting for nearly 40% of reported ADCs [1]. To further improve sampling rates, various techniques for SAR ADCs have been proposed.

Flash-assisted SAR ADCs improve conversion speed by employing a fast flash conversion for the upper bits [7], [8], [9], [10]. However, the flash resolution is typically limited to 3–4 bits, since additional comparators significantly increase power consumption and input loading. Multi-bit-per-cycle SAR ADCs achieve higher conversion speed by resolving multiple bits in each cycle [11], [12], [13], [14]; however, the extra comparators degrade power efficiency compared to single-bit architectures. Pipelined SAR ADCs improve throughput by combining SAR conversion with residue amplification [15], [16], [17], [18], but the residue amplifiers add analog complexity and calibration overhead. In conventional SAR ADCs, the comparator reset phase between conversion cycles limits the operating speed. To overcome this limitation, loop-unrolled (LU) SAR ADCs were proposed [19], [20], [21], [22]. Although employing multiple comparators increases the input loading, the LU SAR reduces the conversion cycle by eliminating the reset phase. To achieve a shorter conversion cycle time, a speculative loop-unrolled (SLU) SAR architecture with an additional CDAC was proposed [23], [24]. To achieve a shorter conversion cycle, the speculative loop-unrolled (SLU) SAR utilizes an additional CDAC to pre-generate the next output voltage before the current comparator decision.

Speculative loop-unrolled (SLU) SAR prototypes have achieved sampling rates above 1.5 GS/s by employing two capacitive digital-to-analog converters (CDAC) in a speculative switching method [23], [24]. Combined with the loop-unrolling technique, the conversion speed is further enhanced without additional comparator power, as the architecture retains single-bit operation. In addition, the design introduces no extra analog complexity or calibration overhead, as all operations are performed entirely in the digital domain. Nevertheless, the speculative approach requires an additional CDAC to be switched speculatively, making the determination of the optimal trade-off between speed and power a key design challenge.

This paper presents an 8-GS/s, 7-bit, eight-way time-interleaved partially speculative loop-unrolled (PSLU) SAR ADC that employs time-domain conversion (TDC) for least significant bit (LSB) generation. The two most significant bit (MSB) conversions are partially speculative, improving conversion speed while reducing power consumption in the CDAC switching logic. All bit conversions are loop-unrolled, and the LSB is resolved simultaneously with the preceding bit through TDC using two additional comparators and SR latches, eliminating the need for an additional conversion cycle and alleviating the noise bottleneck associated with the additional bit. Compared to prior SLU architectures, the proposed design achieves a more favorable speed–power trade-off, enabling efficient multi-GS/s operation. Furthermore, the proposed architecture enables higher per-channel

sampling rates, reducing interleaving complexity for future ADCs operating at several tens of GS/s.

This paper is organized as follows. Section II provides background on the speculative technique. Section III describes the proposed PSLU SAR ADC architecture. Section IV describes the circuit implementation. Section V presents measurement results from a 28-nm CMOS prototype. Section VI concludes the paper.

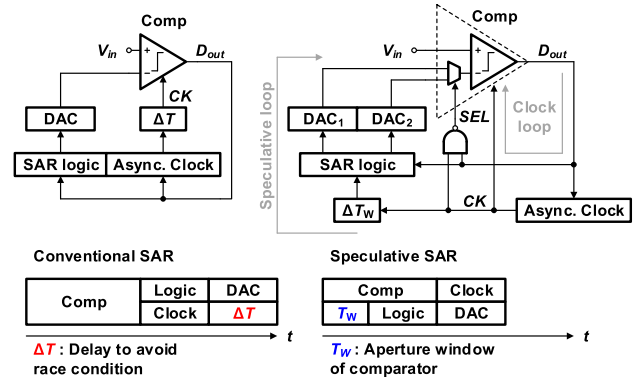


FIGURE 1. Architecture comparison between conventional SAR and speculative SAR.

II. BACKGROUND

As illustrated in Figure 1, a conventional SAR architecture operates asynchronously, with the comparator output directly driving both the SAR logic and the clock generator. Once the comparator decides D_{out} , the SAR logic updates the digital-to-analog converter (DAC), while the clock generator prepares the comparator for the next cycle. To prevent premature activation of the comparator before the DAC has settled, an extra delay of ΔT must be inserted into the clock path. As a result, the minimum achievable loop delay in the conventional SAR for cycle i ($T_{conv,i}$) is defined as follows:

$$\begin{aligned} T_{conv,i} &= T_{comp,i} + \max(T_{logic} + T_{DAC}, T_{CK} + \Delta T) \\ &\geq T_{comp,i} + T_{logic} + T_{DAC} \end{aligned} \quad (1)$$

where $T_{comp,i}$, T_{logic} , T_{DAC} , and T_{CK} represent the comparator delay for cycle i , SAR logic delay, DAC settling delay, and asynchronous clock generation delay, respectively.

In this architecture, the limitation arises from the sequential dependency between the comparator decision and DAC settling. Even if the clock for the subsequent cycle were generated earlier, an additional delay would be required to avoid race conditions. To overcome this sequential limitation, the “speculative” SAR architecture decouples the comparator from the DAC settling by using a latch and two DACs. The latch preserves the current DAC state as long as the aperture window (T_W) to prevent race conditions. The two DACs generate possible outputs corresponding to the comparator decision. The speculative operation proceeds as follows: when CK rises, the comparator performs the comparison based on the current input. After T_W , the SAR logic initiates

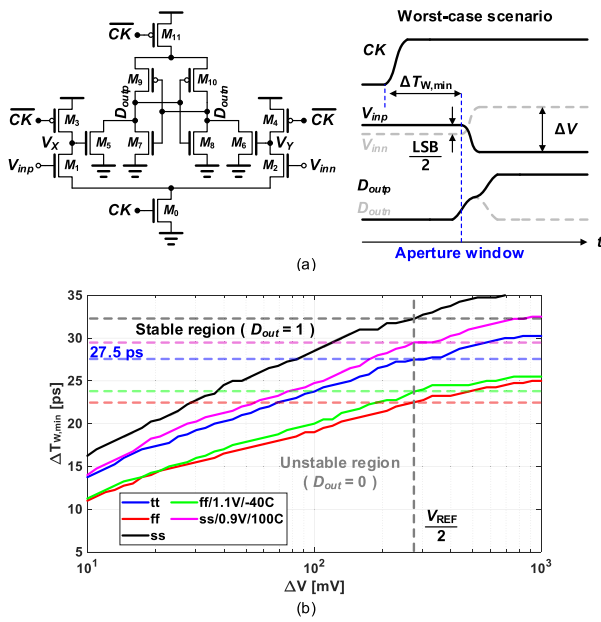


FIGURE 2. Simplified double-tail latch comparator and worst-case scenario in speculative operation, and (b) minimum aperture window required over voltage level to be switched across different PVT corners.

the DAC conversion. Once the decision is complete, it drives the selection logic (NAND gate in Figure 1) to generate SEL signal and select the correct DAC output with the multiplexer for the next cycle. The comparator output also drives the asynchronous clock generator to proceed with the next SAR conversion. As a result, the minimum achievable loop delay in the speculative SAR for cycle i ($T_{spec,i}$) is defined as follows:

$$T_{spec,i} = T_W + T_{logic} + T_{DAC} \quad (2)$$

where T_W represents the aperture window of the comparator.

The key design consideration in the speculative SAR is the aperture window of the comparator. If it is set too short, the DAC updates the current input prematurely while the comparator is still resolving the decision, thus, a race condition occurs. If it is too long, the DAC updates late even though the comparator has made the decision, causing the overall conversion speed to be degraded. The worst-case scenario arises when a small differential input is reversed into a larger input after the aperture window, where the maximum required delay corresponds to the end of the pre-amplification phase [25], [26]. As a result, since the delay of the comparator consists of the sum of the pre-amplification and regeneration delays, the speculative SAR can achieve a speed enhancement up to the regeneration delay per cycle compared to the conventional SAR.

Figure 2(a) illustrates the worst-case scenario in the speculative SAR operation with a simplified double-tail latch comparator. As the CK triggers the comparator, the pre-charged pre-amplification stage outputs (V_X , V_Y) integrate the differential input. After that, the regeneration stage decides the comparator output, as one of M_5 and M_6 turns on

first [26]. With an $LSB/2$ differential input, the SAR operation should retain its current DAC state during the aperture window to prevent the timing violation between the DAC and the comparator. Figure 2(b) shows the minimum aperture window required depending on the voltage level to be switched. As shown in Figure 2(a), since the V_{inp} is higher than V_{inn} , the current bit decision should match this, regardless of the voltage being switched. In the SAR operation, the maximum switching voltage is close to $V_{REF}/2$, thus, the DAC should be switched after a delay of at least 27.5 ps in the speculative SAR operation.

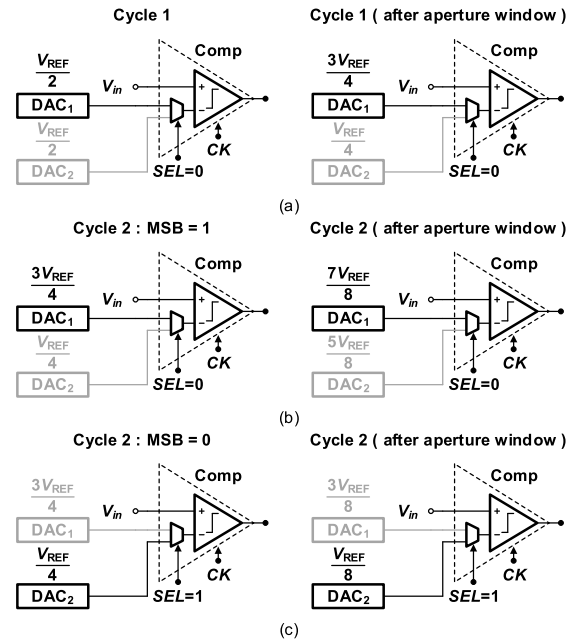


FIGURE 3. Single-ended examples of speculative SAR operation: (a) first cycle, (b) second cycle if MSB equals 1, and (c) second cycle if MSB equals 0.

Figure 3 illustrates single-ended examples of the speculative SAR operation during the first two cycles. The speculative SAR operation is implemented with two DACs and a comparator-embedded multiplexer that is triggered by SEL to select the correctly converted DAC for the next cycle. In the first cycle, both DACs are initialized to $V_{REF}/2$, and the comparator compares the input with the DAC₁ output. After the aperture window, DAC₁ and DAC₂ update their states to the possible outputs corresponding to the comparator decision for the next cycle. As shown in Figure 3(b), if $V_{in} > V_{REF}/2$, the MSB is set to 1, and SEL is set to 0. On the other hand, as shown in Figure 3(c), if $V_{in} < V_{REF}/2$, the MSB is set to 0, and SEL is set to 1. In the second cycle, the SEL selects the DAC which is switched in the correct direction for the next comparison, and the subsequent SAR operation proceeds speculatively. It is important to note that comparator decisions and DAC conversions occur in parallel, separated from the time difference as much as the aperture window of the comparator without violating race conditions.

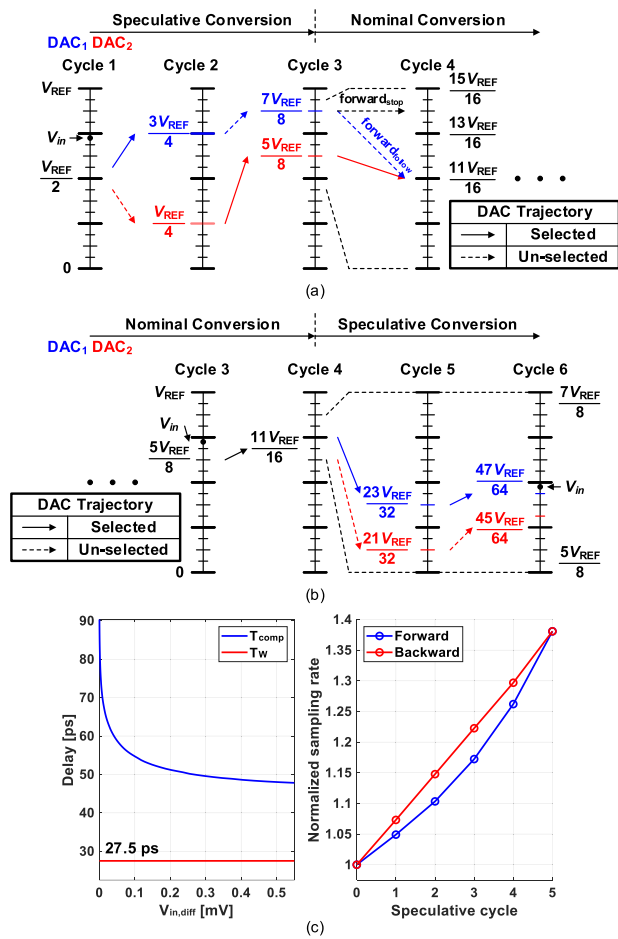


FIGURE 4. Partial speculative concept: (a) forward partial speculative SAR, (b) backward partial speculative SAR, and (c) simulated delays for comparator and aperture window over differential input voltage and sampling rate enhancement over speculative cycles.

III. PROPOSED PSLU SAR ADC

A. PARTIALLY SPECULATIVE SAR

The speculative SAR architecture clearly provides a useful solution to increase the conversion speed of ADCs, but it has two drawbacks. First, the DAC switching energy inevitably increases because the voltage transition in the unselected DAC is larger than in the selected DAC. Second, since the maximum input voltage to be compared varies across cycles, the comparator delay also varies, preventing full speed enhancement through the speculative technique.

To address these limitations, two partial speculative SAR approaches are proposed to balance speed and power efficiency: forward and backward partial speculative SAR. In the forward partial speculative SAR, speculative CDAC switching is applied only to the upper-bit decisions, while the lower-bit decisions are performed in the nominal SAR conversions. Conversely, in the backward partial speculative SAR, the upper bits are resolved by the nominal SAR conversions, and the subsequent conversions are resolved speculatively.

Figure 4(a) illustrates a 2-bit forward partial speculative SAR example for a 6-bit ADC. During the first three cycles, both DACs generate two possible outputs. Afterward, the DAC selected in the final speculative conversion continues with nominal SAR conversions. The forward partial speculation can be further divided into two schemes: forward-stop and forward-follow. In the forward-stop scheme, the unselected DAC ceases switching after the speculative conversion, while in the forward-follow scheme, the unselected DAC tracks the selected DAC output for potential use in subsequent nominal conversions.

Figure 4(b) shows a 2-bit backward partial speculative SAR example for a 6-bit ADC. In this case, both DACs remain at the same level until the fourth cycle, after which speculative conversions are performed in the remaining cycles. It should be noted that DAC outputs are updated to target levels differently, depending on the partial speculative scheme and the input voltage, which significantly affects the overall conversion speed.

To analyze the speed enhancement, the comparator delay and the aperture window are compared as functions of the differential input, as shown in Figure 4(c). While the aperture window, implemented in digital logic to prevent race conditions in the worst-case scenario, remains constant, the comparator delay increases exponentially as the input voltage decreases. By referring the comparator delay look-up table as shown in Figure 2, the expected speed enhancement is estimated for a 6-bit ADC. The sampling rate is normalized to that of a conventional SAR, where the conventional rate corresponds to the case when the speculative cycle is zero. The fully speculative SAR improves the sampling rate by 38%, and the 2-bit partially speculative SARs achieve 10% and 15% improvements in the forward and backward schemes, respectively. The backward scheme provides a higher sampling rate than the forward scheme because the effective input range of the CDAC output decreases progressively as the SAR conversion proceeds, where the regeneration delay increases.

To analyze the power consumption of the partial speculative SAR, the CDAC switching scheme must first be determined. Since the pre-amplification delay in the dynamic comparator varies with the input common-mode voltage, the proposed speculative SAR employs a common-mode balanced CDAC switching scheme to maintain a consistent aperture window in every cycle. The major additional power consumption in the speculative technique is the switching-back mechanism used to update the DACs to their target levels. As shown in Figure 5(a), this switching-back process consumes three times the energy of a nominal CDAC conversion during the speculative conversion. In the forward-stop scheme, additional switching energy is limited to this speculative conversion. The forward-follow scheme requires the same energy as the forward-stop scheme; however, immediately after the speculative conversion, it requires five times the switching energy to track the selected CDAC and consumes the same energy as the selected CDAC for the subsequent cycles. However, in the backward scheme, both

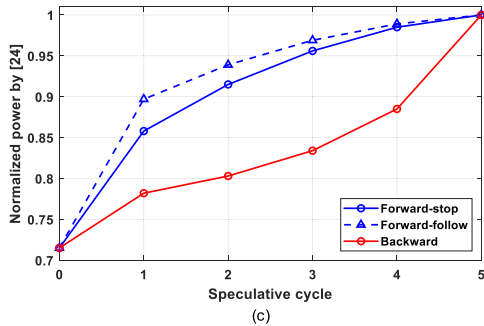
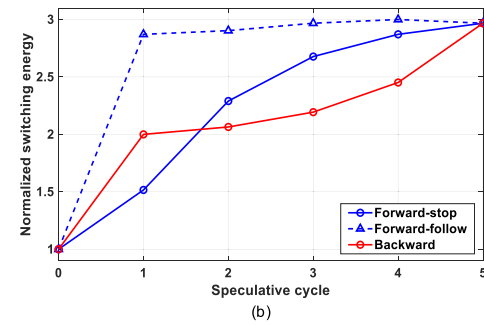
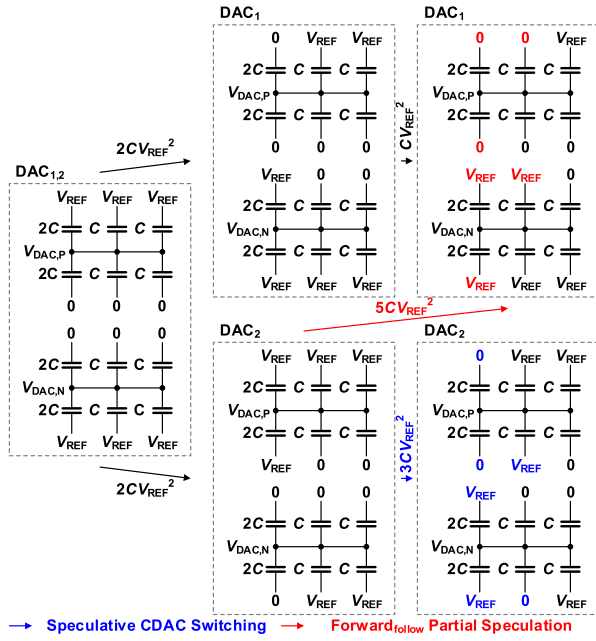


FIGURE 5. (a) Partial speculative CDAC switching example along with switching energy, (b) switching energy comparison for 6-bit conversion and (c) power of the 6-bit ADC normalized to [24].

CDACs initially consume twice the switching energy as in a nominal conversion, and an additional three times the energy due to the speculative conversion.

Figure 5(b) shows the switching energy comparison for the 6-bit partially speculative SAR architecture. The results indicate that the switching energy of the speculative SAR is roughly two to three times higher than that of the non-speculative approach, where the number of speculative cycles is zero. It should be noted that the backward scheme

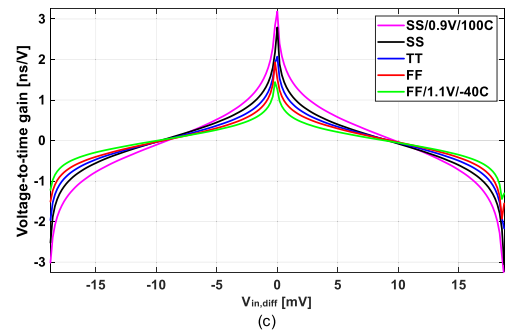
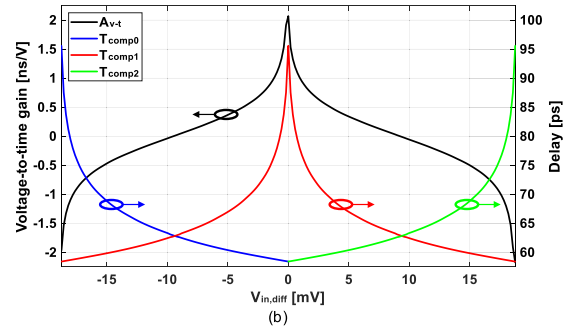
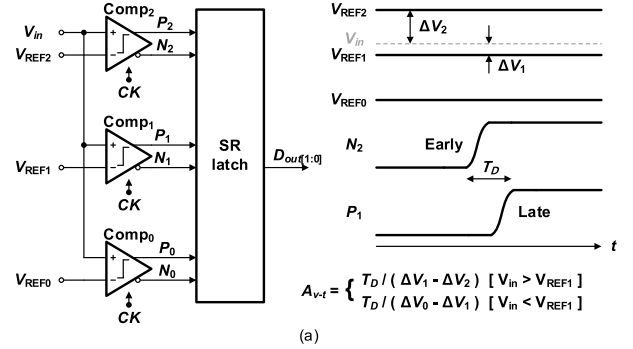


FIGURE 6. (a) 2-bit per cycle architecture with time-domain conversion, and (b) comparator delays and voltage-to-time gain (c) voltage-to-time gain across different PVT corners.

consumes less energy than the forward scheme as the number of speculative cycles increases, because the required capacitance to be converted decreases as the SAR conversion proceeds.

Fig. 5(c) shows the 6-bit partially speculative power consumption normalized to [24]. The results indicate that the forward scheme consumes approximately 10% to 15% more power than the backward scheme, resulting from the sequential decrease in active switching logic as the SAR conversion proceeds.

The proposed PSLU SAR ADC adopts a 2-bit forward-follow partial speculative scheme. Although the backward architecture offers superior speed and power efficiency, it cannot be integrated with the TDC structure that utilizes both CDAC sets for LSB generation. To implement this, both forward-stop and forward-follow configurations must perform switching operations for the final bit. Consequently, while both structures consume identical digital logic power,

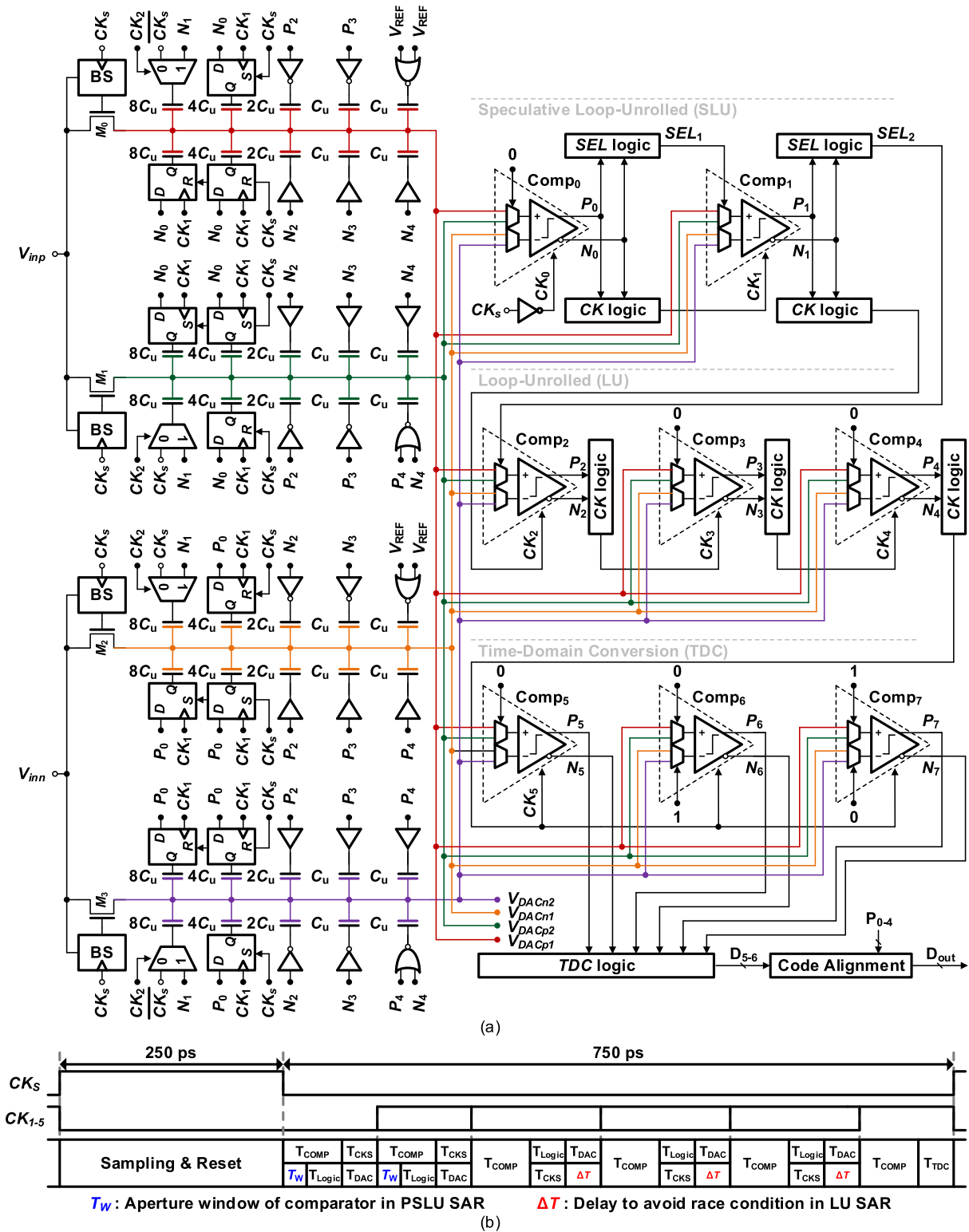


FIGURE 7. (a) 7-bit PSLU SAR implementation with TDC and (b) timing diagrams.

the forward-follow scheme reduces both switching energy and settling time during the LSB transition, making it highly suitable for TDC-compatible designs.

B. TIME-DOMAIN CONVERSION FOR LSB

Increasing the resolution with extra cycles inevitably enlarges the total capacitance and degrades the conversion speed. To

overcome this limitation, a time-domain conversion scheme is proposed in the LSB conversion, which achieves higher resolution without additional cycles or capacitance overhead by employing the dual-CDAC architecture used for the speculative conversion.

As illustrated in Figure 6(a), two additional comparators are incorporated within a single cycle, similar to a multi-bit SAR architecture, enabling simultaneous two-bit generation. Unlike conventional multi-bit SAR conversion requiring precisely divided reference levels such as one-quarter, one-half, and three-quarters of V_{REF} to resolve two bits within a single cycle, the proposed scheme determines the bits by comparing the input only with 0, $1/2$, and $1V_{REF}$. As a result, no additional precise reference generation is required, and the capacitance overhead in the SAR is mitigated. For example, if V_{in} lies between V_{REF1} and V_{REF2} and is closer to V_{REF1} , $Comp_2$ responds earlier than $Comp_1$, producing an early signal. The subsequent SR latch resolves D_{out} by comparing the relative timing of the early and late signals, resulting in 2'b10.

Figure 6(b) shows the voltage-to-time gain (A_{v-t}) of the proposed TDC architecture, derived from the delay difference among the comparators. A larger magnitude of A_{v-t} increases the timing difference between the early and late signals, which is defined as follows:

$$\begin{aligned} A_{v-t} &= T_D / (\Delta V_1 - \Delta V_2) | (V_{in} > V_{REF1}) \\ &= T_D / (\Delta V_0 - \Delta V_1) | (V_{in} < V_{REF1}) \end{aligned} \quad (3)$$

where T_D , ΔV_0 , ΔV_1 and ΔV_2 represent the relative timing between the early and late signals, and the voltage difference between the input and reference voltages, respectively. Figure 6(c) illustrates the variation in voltage-to-time gain across different PVT corners.

As a result, the prototype with the partial speculative and TDC schemes performs 7-bit conversion with the total capacitance required for only six conversion cycles, improving both speed and hardware efficiency.

IV. CIRCUIT IMPLEMENTATION

The structure of the 7-bit unit PSLU SAR ADC and timing diagram are illustrated in Figure 7. It consists of eight dynamic comparators, two CDAC SEL logic, five CK logic, four bootstrapped switches, two differential speculative switching CDACs, and a TDC logic. The first two bits are performed using the 2-bit forward partial speculative SAR with the SEL logic, while all the conversions are executed through loop unrolling. The LSB decision is executed through the TDC scheme that is synchronized to CK_5 .

To implement the aperture window and the switching-back mechanism, reset and set true single-phase clock flip-flops (TSPC_R and TSPC_S) are used for the speculative conversions. The common-mode balanced CDAC switching scheme is implemented with 0.6-fF metal-oxide-metal (MOM) unit capacitors. Only the last conversion uses a monotonic switching scheme that incorporates with the TDC scheme, resulting

in a 32-fF input load including parasitic capacitance from the eight dynamic comparators and bootstrapped switches for each CDAC output.

The proposed 7-bit PSLU SAR ADC architecture employs dual differential CDACs, consequently increasing its sensitivity to component mismatch and degrading the linearity compared to the conventional single CDAC structure. Figure 8 illustrates the behavioral simulation results of the maximum differential nonlinearity (DNL) over 200 iterations with a 1% mismatch applied to each unit cap of the CDAC, yielding a mean of 0.21 LSB and a standard deviation of 0.06 LSB, which are well within the acceptable range of the SAR ADC.

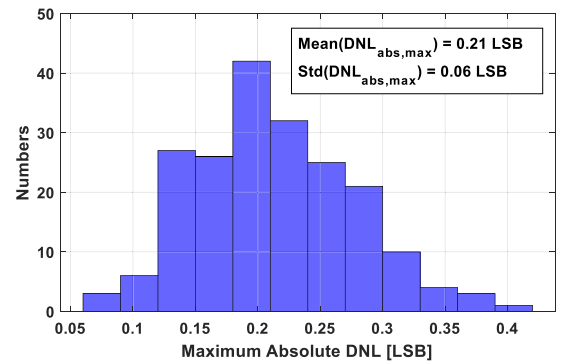


FIGURE 8. Behavioral simulation of the maximum absolute DNL of the proposed 7-bit PSLU SAR ADC with 1% unit cap variation.

A. FOUR-INPUT DOUBLE-TAIL LATCH COMPARATOR

As shown in Figure 9, the dynamic comparators are designed with double-tail latches. To implement the multiplexing mechanism for the two differential CDACs, the design incorporates multi-input branches with four select transistors (M_{0-3}) and four input transistors (M_{4-7}). To address offset voltage and differential current caused by kickback and mismatch, calibration branches replicate the input and select transistor structures. On-chip 6-bit resistive DACs provide the reference voltage, covering a $\pm 3\sigma$ offset range. The comparator offset calibration is performed in foreground with a zero-differential input [24]. Figure 9(b) shows the simulation results of the double-tail comparator, including the comparator delay, aperture window, power, and input-referred noise. The comparators operate with a 550-mV input common-mode voltage and achieve a 1.4-mV_{rms} input-referred noise voltage, satisfying the noise requirement of less than $1/2$ LSB.

The proposed double-tail latch structure minimizes the impact of comparator hysteresis-induced kickback by tying the source of the input transistor to ground rather than to the select transistor, ensuring that the input transistor terminals remain at V_{SS} throughout the decision. Conversely, the conventional structure experiences changes in the terminals, particularly at the source, which accumulate in the CDAC through the kickback and cannot recover because resets occur only during the acquisition time. Figure 9(c) shows the transient noise simulation results of accumulated kickbacks in the CDAC under differential input for 200 cycles. While both

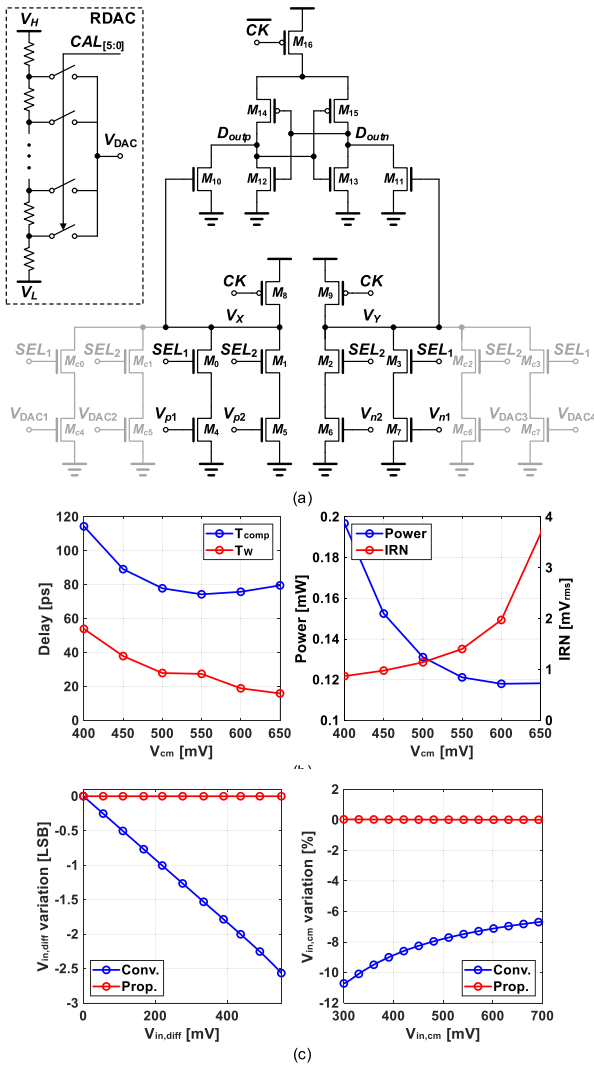


FIGURE 9. a) Double-tail latch comparator, simulation results for (b) overall performances, and (c) differential and common-mode variations by kickback over differential and common-mode input voltage, respectively.

structures exhibit roughly $100\text{-}\mu V_{rms}$ standard deviation, the conventional structure accumulates overall kickback of up to 5 LSB at the end of the fifth conversion in 7-bit architecture, resulting in a dynamic offset that degrades a signal-to-noise-and-distortion ratio (SNDR) by 14 dB. The proposed structure, however, maintains the constant common-mode voltage in every cycle, which prevents performance degradation due to the dynamic offset and the preamplification delay variations. Furthermore, the proposed comparator structure rarely suffers from the common-mode voltage reduction by kickback, preventing race conditions with premature CDAC switching.

B. SPECULATIVE CDAC SWITCHING LOGIC

To implement the speculative switching technique, the CDAC switching logic should be triggered to the clock signals. As shown in Figure 10(a), TSPC D flip flops are implemented

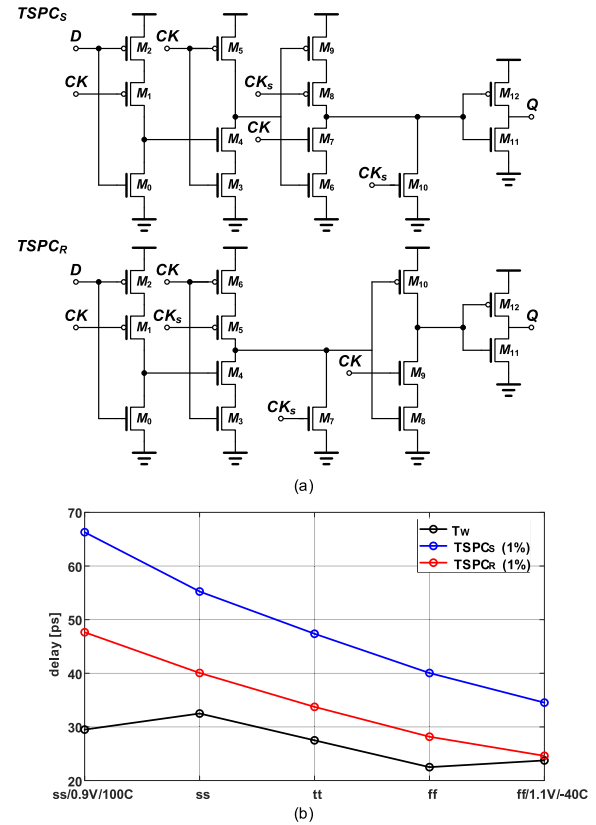


FIGURE 10. a) TSPC/S (reset/set) D flip flop schematic, and (b) simulated comparator pre-amplification delay with 1/2LSB differential input and clock-to-Q delay of TSPC over PVT variations.

in the CDAC switching logic. To implement resetting to CDAC initial states, set/reset transistors are added depending on the initial state. The conversion process is as follows. While the bootstrapped switch is sampling, the flip flops are in the reset phase. After the bootstrapped switch finishes its sampling, all the flip flops hold their initial state except the first conversion and reverse the flip flop outputs connected to $8 \cdot C_u$ to pre-generate target input level for (MSB-1)th conversion as triggered by CLK_S . After that, as the comparator for MSB completes the decision, the generated internal clock triggers the flip flops, and this corresponding process repeats in the subsequential bit conversion.

To verify the flip flops matching the pre-amplification phase of the double-tail latch, clock-to-Q delays and set/reset-to-Q delays should be examined. Figure 10(b) shows the delay comparisons between the comparator pre-amplification and the TSPC over PVT variations. To ensure that the comparator is not disturbed by the CDAC transition, the TSPC propagation delay is set to 1% transition in the final state. The simulation result suggests that the clock-to-Q delay of the designed TSPC consistently exceeds the pre-amplification delays with at least 1 ps. Incorporating with the common-mode balanced CDAC switching, this ensures that race conditions are prevented even for a differential input with 1/2LSB.

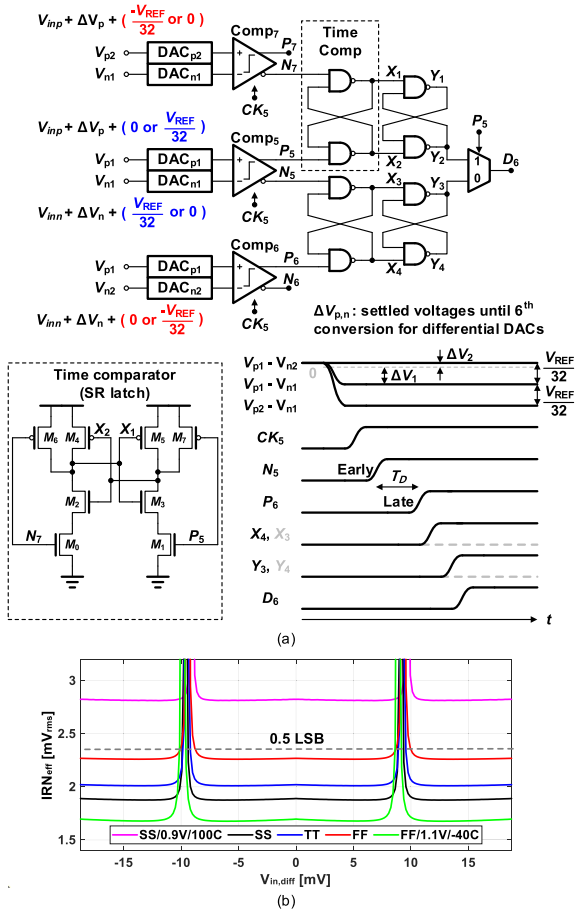


FIGURE 11. (a) TDC implementation, and (b) effective input referred noise over differential input voltage across different PVT corners.

C. TIME-DOMAIN CONVERSION

Figure 11(a) illustrates the LSB decision through time-domain conversion, which employs the unused CDAC₂ and two additional comparators (Comp₆₋₇), along with NAND SR latches. By cross-coupling the two differential CDACs and incorporating monotonic switching in the last CDAC conversion, the reference voltages are generated with the voltage interval of $V_{REF}/32$. For instance, if D_4 equals 1, DAC_{n1} shifts up by $V_{REF}/32$ and DAC_{p2} shifts down by $V_{REF}/32$, while the other DACs remain constant. The three comparators synchronized to the CK_5 produce early and late pulses based on the comparator delays. The SR latches, which serve as time comparators, determine the LSB by comparing the early and late pulses. Depending on the output of Comp₅, only two of the three comparators are used for the LSB decision, and only these two comparators and the SR latches affect the overall noise performance. Thus, the total input-referred noise ($v_{n,total}$) is defined as follows:

$$v_{n,total} = \sqrt{\sum_{i=1}^n (v_{n,comp,i})^2 + \left(\frac{t_{j,latch}}{A_{v-t}}\right)^2} \quad (4)$$

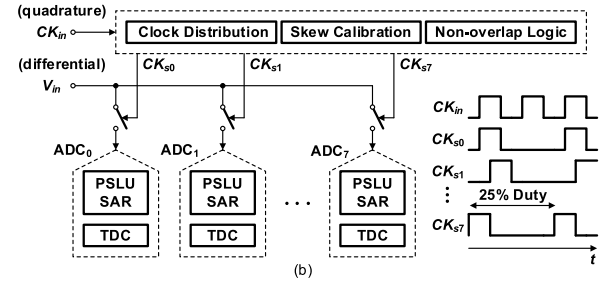
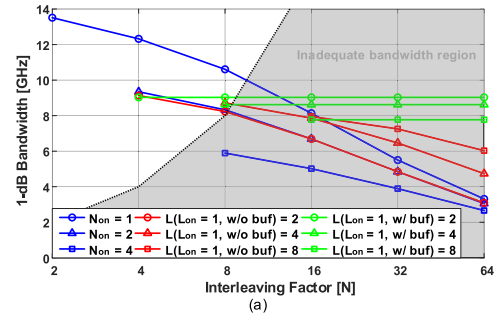


FIGURE 12. (a) 1-dB bandwidth comparison of interleavers, and (b) eight-way time interleaved SAR implementation.

where $v_{n,comp}$ and $t_{j,latch}$ represent the comparator input-referred noise, and the SR latch input-referred jitter, respectively.

Figure 11(b) shows that the jitter in the SR latch contributes approximately 4% of the total input-referred noise compared to the comparators, where 1 LSB is approximately 4.69 mV. The noise increases only when the input is less than 1/2 LSB, where the voltage-to-time gain approaches zero. Thus, the total noise is dominated by the input-referred noise of the comparators, with a requirement of less than 1/2 LSB. Consequently, the effective noise is dominated by the comparator's input-referred noise and increases by a factor of the square root of 3, mitigating the performance degradation typically associated with increased resolution. As shown in figure 6(c), the voltage-to-time gain varies across PVT corners, with the worst-case condition corresponding to reduced timing sensitivity. Nevertheless, the effective resolution remains within the decision margin, ensuring reliable operation. The timing margin is preserved across all evaluated corners.

D. MULTI-CHANNEL DESIGN

Each PSLU SAR, incorporating the TDC for the LSB, achieves 7-bit conversion at a 1-GS/s sampling rate. To further improve the sampling rate, the proposed SAR is implemented with eight time-interleaved channels. In the interleaved architecture, the design must consider the interleaving factor, target sampling rate, and interleaver topology. Voltage-domain interleavers are divided into three types: direct sampling, inline de-multiplexer (de-mux) sampling, and re-sampling [27].

Figure 12(a) shows the 1-dB bandwidth comparison between the interleavers modeled linearly, where N_{on} , L , and

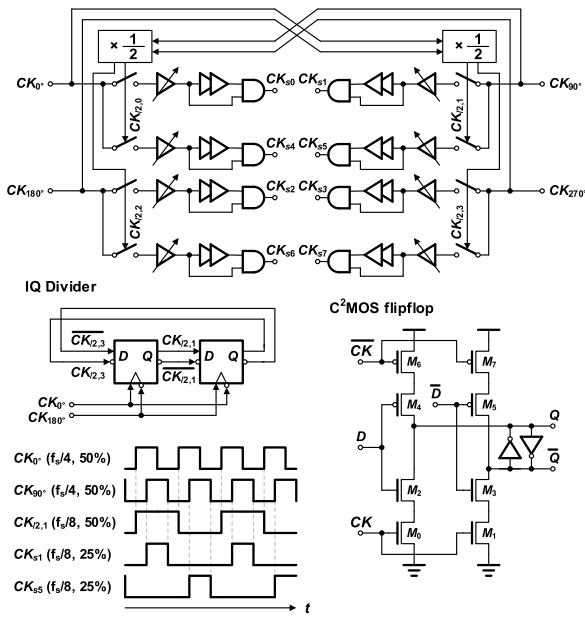


FIGURE 13. Clock generation circuit implementation.

TABLE 1. Noise power breakdown of SAR ADC.

Noise Source	Noise Power [mV ²]	RMS noise [mV _{rms}]	Noise Percent [%]
Quantization Noise	1.831	1.353	32.5%
Clock Network & Sampling Noise*	0.200	0.448	3.6%
CDAC Noise	0.138	0.372	2.5%
Comparator Input-referred Noise**	3.460	1.860	61.4%
Total Noise	5.629	2.373	100%
SNR		39.0 dB	

*With Nyquist input.

**Effective comparator input-referred noise.

L_{on} represent the number of channels sampling concurrently, the number of de-multiplexed channels, and the number of de-multiplexed channels sampling concurrently, respectively. Considering the single-channel conversion speed, all interleaver designs except the direct sampling interleaver with $N_{on}=4$ satisfy the 1-dB bandwidth for the eight time-interleaved channel. To minimize the power consumption and hardware overhead from the interleaver and clock generation circuit, the interleaved architecture employs the direct sampling interleaver with $N_{on}=2$, requiring eight overlapping clocks with a 25% duty cycle, as shown in Figure 12(b).

Figure 13 illustrates the detailed clock generation circuit, providing eight clocks with a 25% duty cycle for the single channel. The circuit consists of two frequency dividers with clocked CMOS logic (C²MOS) flip flops, eight transmission gates, a 4-bit digitally controlled delay line (DCDL) for skew calibration, and non-overlapping logic. By minimizing the number of stages between the input clocks and the channels, the transmission-gate-based architecture effectively reduces

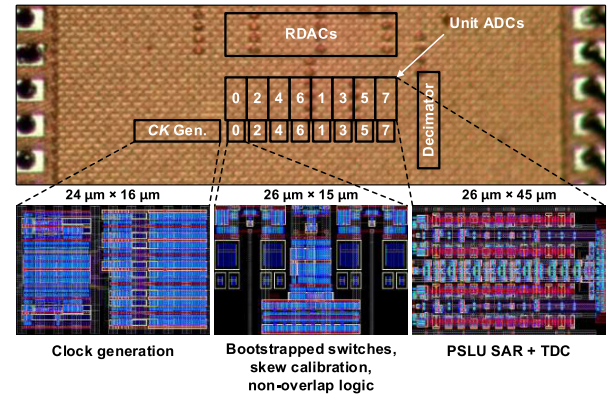


FIGURE 14. Die photograph and detailed layout.

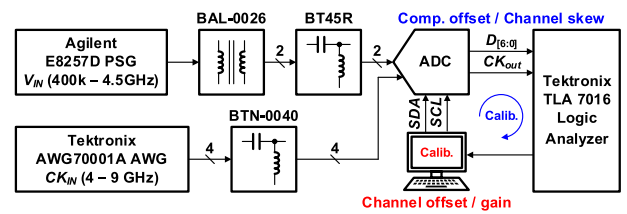


FIGURE 15. Calibration and measurement setup.

pulse error [28]. The IQ divider with the C²MOS flip flops ensures proper alignment between the input clocks and the divided clocks and enhances robustness against phase overlap and race conditions.

Monte Carlo simulation results reveal that the 4-bit DCDL compensates for phase mismatches with a 143-fs delay step, covering up to 6σ . The non-overlapping logic reduces the pulse width by 20 ps to generate pulses so that edges between the clocks in the odd and even channels do not overlap.

Consequently, noise simulation results reveal that the clock generation circuit achieves 44.6-fs_{rms} output jitter, which has a negligible impact on the proposed interleaved SAR operating at the 8 GS/s sampling rate.

E. NOISE POWER BREAKDOWN

Table 1 illustrates the noise power breakdown of the 8 GS/s PSLU SAR ADC with a full-scale Nyquist input. The RMS noise is referenced to a 600-mV_{pp} full scale range. The comparators contribute most noise. With total input-referred noise of 2.373 mV_{rms}, the ADC exhibits a 39.0 dB SNR.

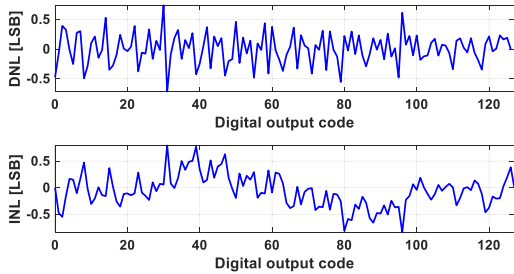
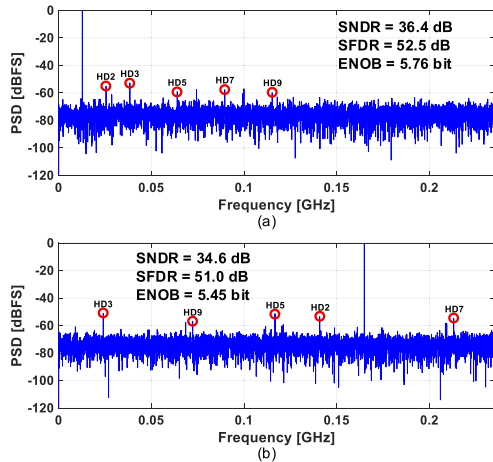
V. MEASUREMENT RESULTS

Figure 14 shows the die photograph and layout of the 7-bit, 8-GS/s prototype, implemented in a 28-nm CMOS process. The active area is 0.013 mm², including the clock generation circuit and the eight-way time-interleaved ADC. Each unit ADC with input switches occupies an area of 26 × 60 μm².

Figure 15 illustrates the calibration and measurement setup for the prototype. In the PSLU SAR, foreground calibrations for comparator offset and clock skew are performed on-chip. These calibrations are executed once prior to measurement

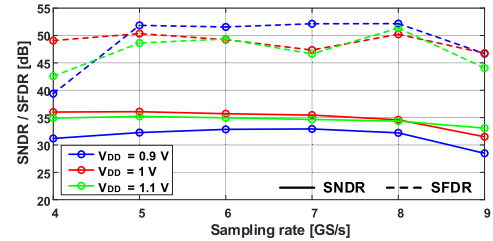
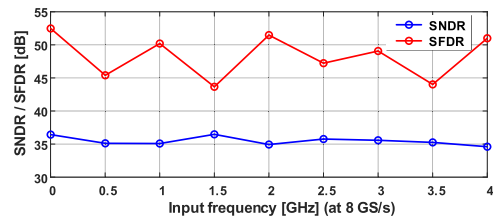
TABLE 2. Performance Comparison With State-Of-The-Art ADCs.

	JSSC'16 [30]	ISSCC'17 [31]	ISSCC'20 [32]	VLSI'21 [33]	VLSI'21 [34]	ISSCC'22 [35]	ISSCC'23 [36]	This work	
Architecture	Hybrid-SAR	SAR	Time-domain	SAR	Time-domain	Time-domain	Time-domain	Hybrid-SAR	
Technology (nm)	28	28 FDSOI	65	16	65	14	28	28	
Resolution (bit)	6	10	8	8	8	8	8	7	
Supply (V)	0.85/ 0.95	1.9/ 1.1/ 0.9	1	0.85	1/ 1.2	0.8	0.9	1	
Channels	16	16	4	8	8	2	1	8	1
Sampling rate (GS/s)	24	8	10	8	20	10	10	8	1
SNDR (dB)	28.9	49.0	40.1	42.4	38.8	37.2	36.4	34.6	35.4
SFDR (dB)	41	60.3	52.8	46	52.5	50.7	51.7	51	49.5
Power (mW)	23	300	50.8	26	129.9	14.8	31.7	19.7	2.06
FoM _W (fJ/cs)	42	162.9	61.5	30.2	90.9	24.8	58.7	56.1	42.8
FoM _S (dB)	146.1	150.2	150	154.3	147.7	152.5	148.4	147.7	155.3
Area (mm ²)	0.03	0.184	0.095	0.023	0.22	0.003	0.009	0.013	0.0016

FoM_W = Power / (sampling rate · 2^{ENOB})FoM_S = SNDR + 10 · log (2 · sampling rate / Power)**FIGURE 16. ADC static characterization: DNL and INL.****FIGURE 17. ADC output spectra after on-chip (comparator offset and skew) and off-chip (channel offset and gain) calibration for (a) f_{in} = 12.8 MHz and (b) f_{in} = 3.9296 GHz at 8 GS/s, decimated by 17, using a 10000-point FFT.**

and can be periodically repeated during system idle phases for practical applications. In contrast, channel offset and gain calibrations are performed off chip through post-processing on a PC.

Figure 16 shows the static characterization of the prototype, including the DNL and integral nonlinearity (INL)

**FIGURE 18. Measured SNDR and SFDR versus sampling rate.****FIGURE 19. Measured SNDR and SFDR versus input frequency at a sampling rate of 8 GS/s.**

measured with a 600-mV_{pp} input swing at a 550-mV common-mode level. The maximum DNL and INL are +0.74/−0.72 LSB and +0.79/−0.84 LSB, respectively.

Fig. 17 shows the decimated (17x) output spectra of the ADC, achieving an SNDR/spurious-free dynamic range (SFDR) of 36.4/52.5 dB for a low-frequency sinusoidal input and 34.6/51.0 dB for a Nyquist-frequency sinusoidal input. The second harmonic (HD2) observed in the time-interleaved ADC output is primarily attributed to a dominant contribution from a specific sub-ADC channel, indicating residual even-order nonlinearity in that channel. The higher-order harmonic components (HD5-HD9) are mainly limited by the finite calibration resolution and residual mismatch in the dual-CDAC architecture, while intrinsic sub-ADC nonlinearity may also contribute.

Figure 18 shows the measured SNDR and SFDR versus the sampling rate under different supply voltages,

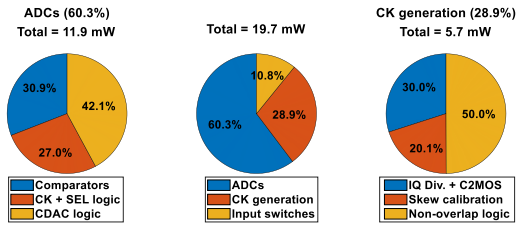


FIGURE 20. Proposed ADC power breakdown.

demonstrating that the prototype maintains an SNDR of approximately 35 dB across sampling rates from 4 to 8 GS/s.

Figure 19 shows the measured SNDR and SFDR versus the input frequencies. The degradation in SFDR exhibits periodic behavior, decreasing and increasing with input frequency, repeating every 1 GHz, consistent with the Nyquist frequency of the unit ADC. Due to the nonlinearity of the input switches, the worst-case distortion is observed at an input frequency of 1.5 GHz, where the SFDR is 43.7 dB, which is sufficient to meet the 35 dB SNDR target, considering internal noise, circuit nonidealities, and measurement constraints such as phase noise and jitter.

Figure 20 provides the power breakdown of the proposed ADC, which consumes a total of 19.7 mW at the 1-V supply voltage and 8-GS/s sampling rate.

Table 2 compares the performance of the proposed PSLU SAR ADC with state-of-the-art ADCs operating at sampling rates above 8 GS/s. By employing the speculative technique and the TDC scheme, the proposed SAR ADC prototype achieves a competitive sampling rate and SNDR. This results in Walden and Schreier figure-of-merit (FoM_W and FoM_S) comparable to other competitive designs. Although the time-domain ADC in [35] reports a higher SNDR, it is PVT-sensitive and requires extensive delay calibration, increasing power consumption and delay-line jitter. In contrast, the proposed SAR ADC incurs minimal overhead for comparator calibration, offering a more robust solution without degrading power or noise performance.

VI. CONCLUSION

This paper presents an 8-GS/s, 7-bit, eight-way time-interleaved PSLU SAR ADC with a TDC. The proposed ADC employs a speculative technique to improve the conversion speed by operating the comparator decision and CDAC settling in parallel. A 2-bit forward partial speculation and TDC scheme are employed to achieve an optimal trade-off between speed and power consumption by reducing the hardware overhead associated with the CDACs. The 7-bit prototype achieves a sampling rate of 8 GS/s with an SNDR of 34.6 dB, an SFDR of 51.0 dB, and figures of merit of 56.1 fJ/conversion-step and 147.7 dB.

While conventional tens-of-GS/s ADCs utilize extensive time-interleaving, this work demonstrates an 8-GS/s core. Incorporating a dedicated interleaver stage can scale the interleaving factor to achieve higher sampling rates. In this configuration, the interleaver architecture governs an

intrinsic power-bandwidth trade-off, which is reserved for future work.

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