

Doping-less tunnel field-effect transistors by compact Si drain frame/Si_{0.6}Ge_{0.4}⁻ channel/Ge source

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ABSTRACT

Tunnel field-effect transistors (TFETs) have attracted immense interest as a promising alternative to complementary metal–oxide semiconductors for low-power-consumption applications. However, conventional TFETs introduce both random dopant fluctuations and ambipolar current issues at negative gate voltages for sub-6-nm technology nodes. In this study, we address the performance of charge plasma-driven doping-less TFETs, including sub-3-nm thick compact drain (CD) geometry/SiGe-channel/Ge source layers for suitable bandgap engineering. An ultrathin CD frame and heteromaterials are adopted for use as channels/sources to improve the ambipolarity and ON-state features, respectively. Simulation demonstrates a clear reduction in the ambipolar current from 3.3×10^{-14} to 3.0×10^{-17} A at gate (V_G)/drain (V_D) voltages of $-1.5/1.0$ V and an enhancement in the ON-current from 2.0×10^{-5} to 8.6×10^{-5} A at $V_G = 1.5$ and $V_D = 1.0$ V, compared with conventional TFETs. In addition, diverse fabrication-friendly metals applicable to industry fieldwork sites are tested to determine how the metal work functions influence the outputs. The use of Ti/W/Ni as the drain/channel/source materials, respectively, yields an enhanced ambipolar current of 1.2×10^{-20} A and an ON-current of 3.9×10^{-5} A.

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Metal-Oxide-Semiconductor-Field Effect Transistors (MOS-FETs) have been the subject of intense focus for fabricating advanced integrated circuits, including those consistently reducing in sizes, up to a sub-10-nm technology node. However, two issues remain as crucial challenges in extending their use for advanced future logic devices: extremely low energy consumption and high switching speeds. Thus, the recently developed multi-gate nanowire FET and double-gate MOSFET with 2D-transition metal dichalcogenide (TMD) channel materials have yielded outstanding subthreshold

swing (SS) performance, close to 60 mV/decade. However, as the next sub-6-nm technical node requires an SS of less than sub-60 mV/decade, tunneling field-effect transistors (TFETs) based on band-to-band tunneling (BTBT) phenomena have emerged as an alternative owing to their considerable advantages of low power consumption and extremely low SS.¹

The conventional TFET is composed of an n⁺-drain/intrinsic channel/p⁺-source, achieving an SS value of less than 60 mV/decade.^{2–5} However, as device geometries have shrunk,

the scaling of conventional TFETs is restricted by the presence of random dopant fluctuations^{6–8} (RDFs); this was found to cause a variation in the threshold voltage (V_T) and SS during the doping and activation process of drain/source regions frequently adopted in conventional TFETs. In addition, conventional TFETs resulted in a higher ambipolar current mainly because of the inherent BTBT phenomena between the drain/channel in the gate voltage (V_G) range being lower than 0 V, even though an ambipolar current⁹ is strongly correlated with stable device operation. Thus, numerous studies have been conducted to address the aforementioned issues of RDF and high ambipolar currents. Utilizing charge plasma-based doping-less (DL) TFETs (DL-TFETs),^{10,11} which employ a rectifier concept without doping, is the predominant method of addressing RDF. Ambipolar current in DL-TFETs can be suppressed via a drain-engineering process, for example, insertion of a metal splint into the drain region toward the gate to increase the length between the gate/drain and adjustment of the drain metal work function.^{12–16} The recent approach for enhancing the ON-current in DL-TFETs is to utilize a source-engineering concept, including heterojunction materials with a lower bandgap energy (E_g) than silicon materials in the source region.^{17–21} However, both conventional approaches have reflected the huge fabrication cost requirements due to multiple lithography–etch–lithography–etch process steps and difficulty in the current sub-10-nm technology node.^{22,23}

Thus, the crucial concepts in this work start with a compact drain (CD) geometry for the advancing ambipolar current feature and the choice of heteromaterials (HMs) of the $\text{Si}_{0.6}\text{Ge}_{0.4}$ -channel/Ge source for improved ON-current, as shown in Fig. 1. This work also tests a diverse range of metal electrodes applicable to the currently available Si-based MOSFET manufacturing process to minimize the number of fabrication steps in the near future. Figure 1(b) shows the AA'-line cross-sectional views of the proposed CD-HM-DL-TFET. As seen in this figure, the CD-DL-TFET exhibits ultrathin silicon (3 nm thick) in the drain region for the suppression of high ambipolar currents frequently observed from conventional DL-TFETs. The HM-DL-TFET exhibits Ge/ $\text{Si}_{0.6}\text{Ge}_{0.4}$ layers in the source and channel regions for the enhancement of ON-current features. For convenience, four devices serving as comparison are denoted as the conventional DL-TFET (device A), CD-DL-TFET (device B), HM-DL-TFET (device C), and CD-HM-DL-TFET (device D), depending on the configuration. First, all devices employed Hf/W/Pt metals serving as drain/channel/source electrodes, respectively. These metals have work functions of 3.9, 4.5, and 5.9 eV, respectively, thereby resulting in the following carrier concentrations: an n^+ -drain of $2.1 \times 10^{18} \text{ cm}^{-3}$, n^- -channel of $7.2 \times 10^{13} \text{ cm}^{-3}$, and p^+ -source of $2.0 \times 10^{19} \text{ cm}^{-3}$, respectively, for the 10 nm thick silicon (see Fig. S1 in the supplementary material). More detailed parameters of devices A, B, C, and D are listed in Table I. Other specific parameters are applied to all devices, where the drain length, gap between the drain and the gate ($L_{g,D}$), gate length, gap between the gate and the source ($L_{g,S}$), and source length are 32, 15, 50, 3, and 44 nm, respectively. The carrier concentration (n_i) of Si, $\text{Si}_{0.6}\text{Ge}_{0.4}$, and Ge is $1.0 \times 10^{15} \text{ cm}^{-3}$ with an intrinsic body. All simulations were conducted using a SILVACO TCAD software tool. In this simulation, a non-local BTBT carrier probability is introduced for determining the variation in the spatial distribution of the band structure and the narrowing²⁴ effect in a forbidden band, together with adapting Shockley–Read–Hall composite and

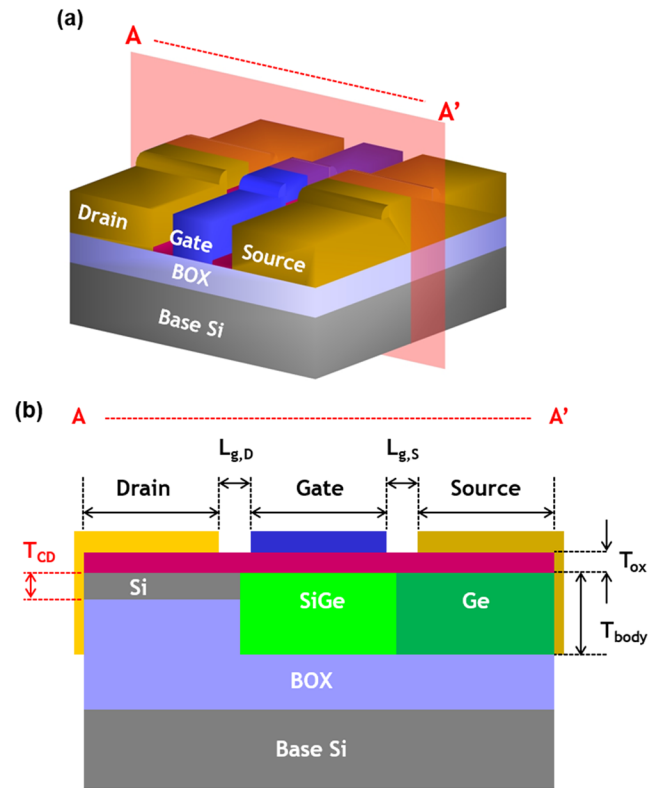


FIG. 1. (a) Schematics and (b) the AA'-line cross-sectional view of the proposed doping-less CD-HM-DL-TFET device (device D) with a compact Si drain and SiGe channel/Ge source (HM) frames.

non-local BTBT models²⁵ for the presence of traps. The Lombardi mobility,²⁶ concentration, and field-dependent mobility models are also considered to accurately calculate the carrier mobility by employing the Fermi–Dirac statistics and bandgap narrowing models for the operation of heavily doped regions.

It is well known that the TFET is expected to produce a higher ON-current at a relatively low V_G than the MOSFET as the tunneling current is highly associated with the following transmission probability (T_{WKB}) approximation^{27,28} of the inter-band tunneling barrier:

$$T_{WKB} \approx \exp\left(-\frac{4\sqrt{2m^* \cdot E_g^3}}{3q\hbar\epsilon}\right), \quad (1)$$

where ϵ is the electric field in the junction, m^* is the effective mass, and E_g is the bandgap. Equation (1) implies that the use of a high bandgap and electric field reduces and increases T_{WKB} , respectively. Thus, the heterojunction containing E_{g1} (SiGe) and E_{g2} (Ge), where E_{g1} (SiGe) is larger than E_{g2} (Ge), supports the presence of an electric field higher than that of the homojunction with only E_{g1} . In addition, the heterojunction must consider both triangular and trapezoidal barriers²⁹ created by two energy bandgaps occurring at junction interfaces,

TABLE I. Detailed parameters of devices A–D for comparison. Boldface denotes the proposed CD-HM-DL-TFET.

		Drain	Gate/channel	Source
Metal electrode (work-function)		Hf ($\Phi_D = 3.9$ eV)	W ($\Phi_G = 4.5$ eV)	Pt ($\Phi_S = 5.9$ eV)
Dielectric (thickness)		SiO ₂ (30 Å)	HfO ₂ (20 Å)	SiO ₂ (5 Å)
Body material (thickness)	Device A	Si (10 nm)	Si (10 nm)	Si (10 nm)
	Device B	Si (3 nm)	Si (10 nm)	Si (10 nm)
	Device C	Si (10 nm)	SiGe (10 nm)	Ge (10 nm)
	Device D	Si (3 nm)	SiGe (10 nm)	Ge (10 nm)

$$T_t = \exp \left\{ -\frac{4\sqrt{2m^*}}{3q\hbar} \left(\frac{E_{g1}^{\frac{3}{2}}}{\mathcal{E}_1} + \frac{E_{g2}^{\frac{3}{2}}}{\mathcal{E}_2} - \frac{(E_{g1} + \Delta E_c)^{\frac{3}{2}}}{\mathcal{E}_2} \right) \right\}. \quad (2)$$

The above-mentioned transformation equation represents the tunneling approximation for the heterojunction having front triangular and rear trapezoidal barriers before/after band off-sets, respectively. For example, the first term of Eq. (2) reflects the triangular tunneling barrier of the channel material, and the second and third terms correspond to the trapezoidal barrier of the source region. Two configurations are chosen for the drain/channel/source layers—Si/Si/Si and Si/Si_{0.6}Ge_{0.4}/Ge—where the electric fields and maximum BTBT rates of each configuration are monitored for devices A, B, C, and D.

Figure 2 plots the silicon thickness-dependent ambipolar characteristics of devices A (black) and B (blue), where devices A and B have silicon thicknesses of 10 and 3 nm in the drain regions, respectively. As seen in Fig. 2(a), the 3 nm thick Si in the drain region of device B increases the energy bandgap (E_g). For example, the E_g of device B (1.27 eV) was larger than that of device A (1.12 eV), as seen in the inset of Fig. 2(b). The presence of a larger E_g in device B is likely due to the conduction-band-minimum and valance-band-maximum shift owing to the quantum-confinement effect arising mainly from the <3-nm-thick Si.^{30,31} The energy band diagrams at a gate voltage (V_G) of -1.5 V and a drain voltage (V_D) of 1.0 V between devices A and B exhibited a widening junction between the drain/channel regions [Fig. 2(a)]. The electric fields in the drain/channel junction for devices A and B were determined to be 9.8×10^5 and 9.3×10^5 V/cm while the maximum BTBT rates were 1.59×10^{23} #/cm³ s and 1.08×10^{21} #/cm³ s, respectively. These observations imply a lower tunneling probability of device B, thus corresponding to a reduction in ambipolar currents of device A from 3.3×10^{-14} to 2.4×10^{-16} A, where $V_G = -1.5$ V and $V_D = 1.0$ V, as evident in Fig. 2(b), i.e., increasing E_g in the drain regions contributes to the advancing ambipolar characteristics.

To identify the ON-current characteristics of devices A and C, Si/Si_{0.6}Ge_{0.4}/Ge are used as the drain/channel/source regions for device C (Fig. 3). As seen in this figure, device C revealed an E_g of 0.84 and 0.67 eV in the channel and source regions, respectively, which are lower than that of silicon (1.12 eV). The energy band diagram of device C recorded at $V_G = 1.5$ V and $V_D = 1.0$ V also yielded a narrowing junction between the channel/source regions [Fig. 3(a)]. The electric fields in the drain/channel junctions of devices A and C at $V_G = 1.5$ V and $V_D = 1.0$ V were 2.6×10^6 and 3.2×10^6 V/cm, while the maximum BTBT rates were

4.25×10^{32} and 1.17×10^{33} #/cm³ s, respectively. Thus, the resulting ON-currents of devices A and C varied from 2.0×10^{-5} to 9.6×10^{-5} A at $V_G = 1.5$ V and $V_D = 1.0$ V, as evident in Fig. 3(b). Such an enhancement to the ON-current of device C implies the

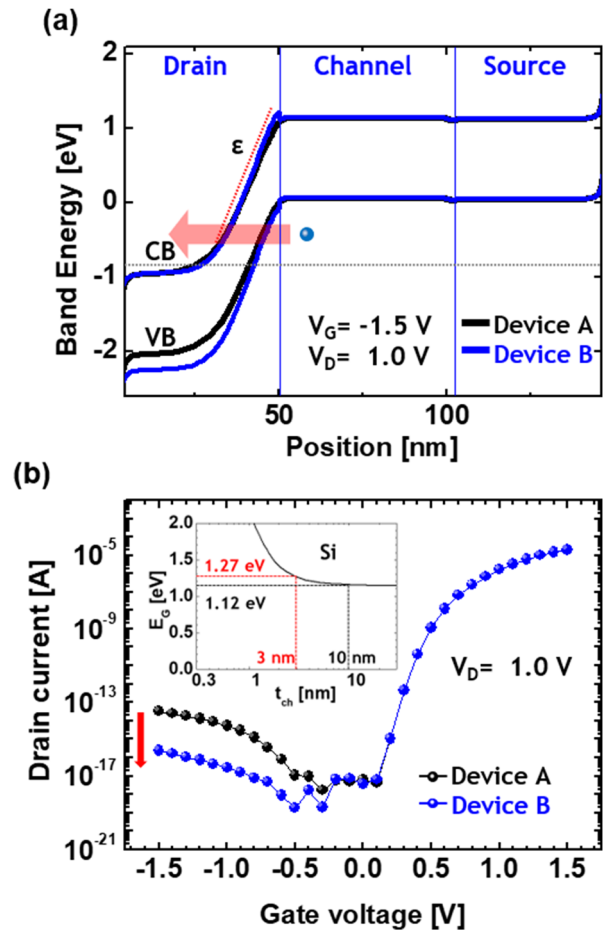


FIG. 2. (a) Energy band diagrams at $V_G = -1.5$ V and $V_D = 1.0$ V and (b) I - V responses of devices A (black) and B (blue), where the inset of Fig. 2(b) shows the variations in the energy bandgap from 1.15 to 1.27 eV, for thicknesses of 10 and 3 nm. The compact drain (CD) configuration of device B leads to a reduction in ambipolar current.

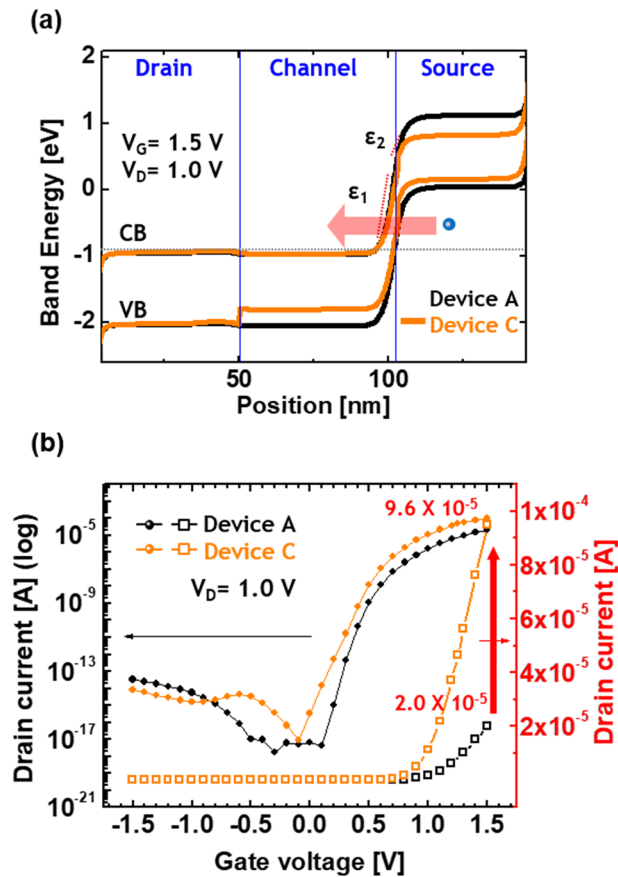


FIG. 3. (a) Energy band diagrams taken at $V_G = 1.5$ V and $V_D = 1.0$ V and (b) corresponding I - V responses of devices A (black) and C (yellow), where the left axis of (b) corresponds to a drain current in a linear-scale. Enhancement to the ON-current of device C is observed by employing the SiGe channel and the Ge source frame.

presence of a high electric field and advanced BTBT rate between the channel/source regions when materials with lower E_g s are applied to the channel/source regions.

To further clarify both the ambipolar and ON-current characteristics observed from devices B and C, device D—with a 3 nm thick Si drain/Si_{0.6}Ge_{0.4}-channel/Ge source configuration—was also evaluated. Figures 4(a) and 4(b) show the plot of the energy band diagrams of devices A (black) and D (red) for ambipolar and ON-current states recorded at $V_G = -1.5$ V and $V_G = 1.5$ V, respectively. For the ambipolar state, the electric fields between the drain/channel regions of devices A and D were 9.8×10^5 and 9.0×10^5 V/cm, respectively, and the maximum BTBT rates were 4.25×10^{32} and 1.17×10^{33} #/cm³ s, respectively. These results are in good agreement with the I - V responses shown in Fig. 4(c). The ambipolar current of devices A and D was 3.3×10^{-14} and 3.0×10^{-17} A at $V_G = -1.5$ V and $V_D = 1.0$ V, whereas the ON-current of devices A and D was 2.0×10^{-5} and 8.6×10^{-5} A at $V_G = 1.5$ V and $V_D = 1.0$ V, respectively. In this work, the observations for device D support enhancement of both the ambipolar current (1.1×10^3 times lower) and

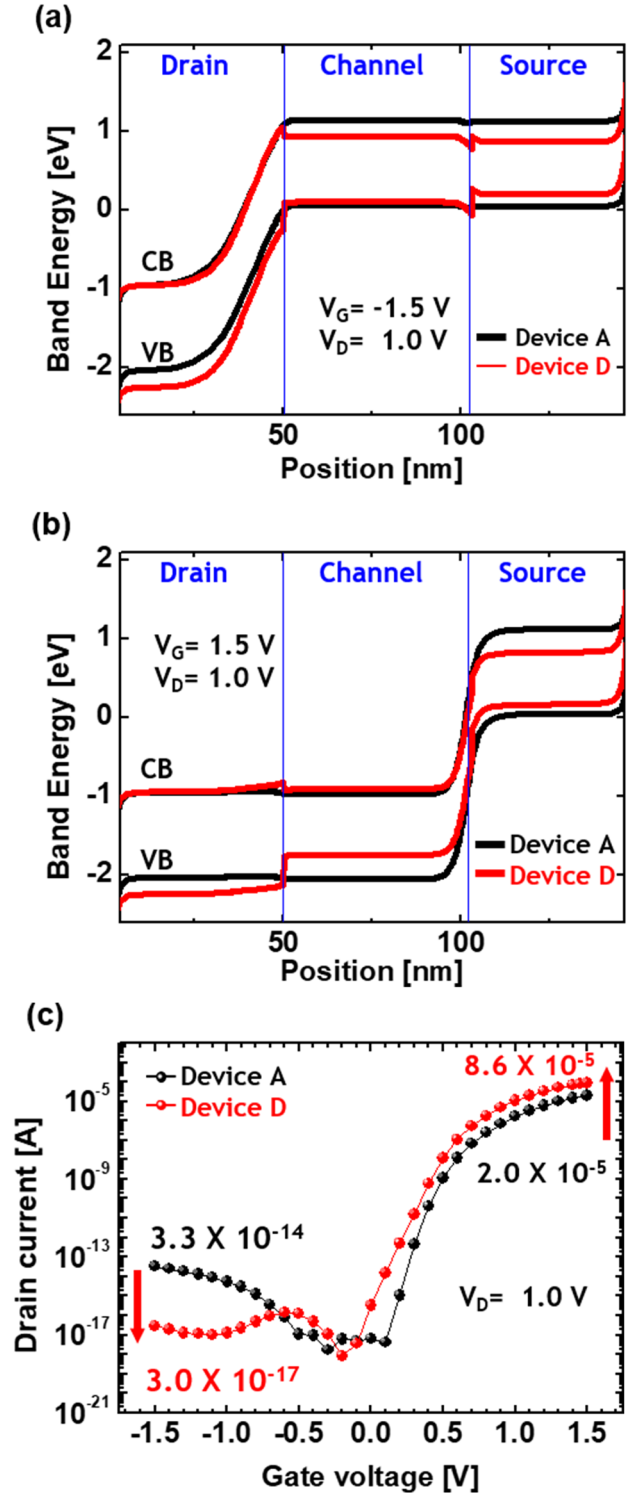


FIG. 4. Energy band diagrams (a) at $V_G = 1.5$ V/ $V_D = 1.0$ V and (b) $V_G = -1.5$ V/ $V_D = 1.0$ V of devices A (black) and D (red). (c) Their corresponding I - V responses. Suitable use of both CD and SiGe channel/Ge source frames reduces the ambipolar current and enhances the ON-current, respectively.

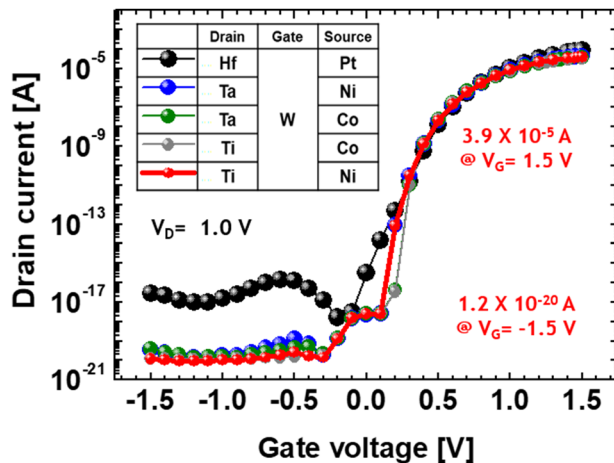


FIG. 5. Contributions of the diverse drain/channel/source metal work function to I - V responses of device D: Hf/W/Pt (black), Ta/W/Ni (blue), Ta/W/Co (green), Ti/W/Co (magenta), and Ti/W/Ni (red).

ON-current (4.3 times higher) by employing a suitable sub-bandgap engineering approach, compared with those of device A serving as a conventional DL-TFET.

To gain possible insight into the potential electrode contributions to the I - V features of device D, fabrication-friendly metals applicable to actual industry fieldwork sites are also tested. As described above, all previous devices have examined the well-known Hf/Pt materials as drain/source electrodes owing to their high carrier concentrations. However, the most practical Si-MOSFETs have chosen electrodes with high conductivity and low diffusivity, including Ta, Ti, Ni, and Co, as listed in the inset table of Fig. 5. Thus, the following metals were chosen as electrodes: Ta (4.25 eV)/Ti (4.33 eV) as drain metals, Ni (5.15 eV)/Co (5.00 eV) as source metals, and W (4.5 eV) as the gate metal; the values in parentheses represent the work function of each metal. Figure 5 exhibits the representative I - V responses of four electrode combinations: Ta/W/Ni (blue), Ta/W/Co (green), Ti/W/Co (gray), and Ti/W/Ni (red). As shown in Fig. 5, the Ti/W/Ni (red) combination yielded a prominent ambipolar current (1.2×10^{-20} A at $V_G = -1.5$ V) and ON-current (3.9×10^{-5} A at $V_G = 1.5$ V), when compared with those of other electrode combinations. Such an enhancement in the ambipolar current for the Ta/Ti drain metals is mainly due to a low work-function difference between Si and Ta or the Ti drain metal, compared with those of the previous Hf metal. The Ta or Ti drain metals provided electron concentrations of 1.1×10^{16} and 5.8×10^{14} cm $^{-3}$, respectively, which were lower than that of the Hf metal (2.1×10^{18} cm $^{-3}$).

In conclusion, we introduce the CD frame and HM layers for the enhancement of both ambipolar and ON-currents through proper band-engineering approaches in conventional DL-TFETs. The CD concept of less than 3 nm thickness reflects an increase in the energy bandgap arising from the conduction-band-minimum and valance-band-maximum shift by quantum-confinement. The choice of HM materials is proven to establish a smaller energy bandgap than the drain and source regions. The proposed device D established the eligibility for attaining advanced performance, such

as a low ambipolar current close to 10^{-21} A, SS of 53.4 mV/decade, V_{DD} of 0.59 V, and I_{on}/I_{off} of 3.25×10^{15} . Thus, we anticipate that the ability to manipulate bandgap engineering in conventional DL-TFETs may lead to practical applications, even though experimental works are necessary to verify the above-mentioned theoretical findings.

See the [supplementary material](#) for cross-sectional schematics and their corresponding carrier concentrations of devices A–D.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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