



Materials and design strategies for interposer-based packaging: A comparative review of silicon, glass, and organic platforms

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ABSTRACT

In heterogeneous integration packaging, interposers are fundamental components that provide high bandwidth, low latency, and die-to-die connections by integrating multiple functional dies, such as logic and memory, within a single package. They have also gained significant attention for addressing challenges that are increasingly difficult to resolve through process scaling alone, such as rising power density, declining reliability, and memory walls. Packaging technologies are expected to become increasingly miniaturized and integrated as the demand for high-performance computing continues to increase in the fields of artificial intelligence, big data, and data center systems. Interposers provide high-density, die-to-die interconnects by combining fine-pitch wiring with through-via and through-via-less connections. In this review, we compare and summarize silicon, glass, and organic interposer technologies from material and structural perspectives, and discuss future research directions and applications, considering the advantages and limitations of each approach.

1. Introduction

Recently, the semiconductor industry has witnessed strong demand for highly integrated, high-performance devices driven by applications such as artificial intelligence and big data [1]. Moore defined Moore's law, which states that the number of transistors that can be integrated on a semiconductor chip approximately doubles every two years [2]. This empirical trend has long revealed the rapid pace of technological advancement in industry. As transistors have been scaled down to the nanometer scale [3], the integration density has increased. However, power consumption, thermal management, and reliability concerns have become more severe. In addition, short-channel effects and lithography limits, including diffraction, have made it increasingly challenging to comply with performance-scaling requirements through transistor size reduction alone [4,5]. The memory wall has also intensified [6]. To overcome these limitations, packaging technologies have evolved beyond their traditional role of protecting chips and emerged as key enablers of high-density interconnectivity and heterogeneous integration [7]. A wide range of advanced packaging approaches exist, including single-die and multi-die packaging [8]. Multi-die packaging has emerged as a promising solution that can simultaneously improve

bandwidth, power efficiency, and integration density. Fig. 1 conceptually summarizes the evolution of high-density packaging architecture. An early example of multi-die packaging is the multichip module technology developed in the 1980 s, in which multiple dies were mounted on a single substrate, enabling shorter interconnect lengths and improved reliability [9]. This concept subsequently evolved into a system-in-package (SiP), which integrates multiple functional components within a single package and enables heterogeneous devices to be combined at the package level, offering an alternative path to monolithic system-on-chip integration [10]. However, such architecture provides limited integration density and bandwidth, motivating more advanced packaging schemes with finer pitch and higher density interconnect structures. In this context, the lateral integration of multiple chips on a package substrate or fan-out redistribution layer (RDL) substrate is referred to as 2D integrated circuit (IC) integration. When the RDL is formed on top of the package substrate, the architecture is termed as 2.1D IC integration. When embedded bridges are incorporated within the package substrate or within the fan-out epoxy molding compound, this is referred to as 2.1D IC integration with bridges. When multiple chips are supported by an inorganic or organic material through-via-less interposer and subsequently attached to a package substrate, the

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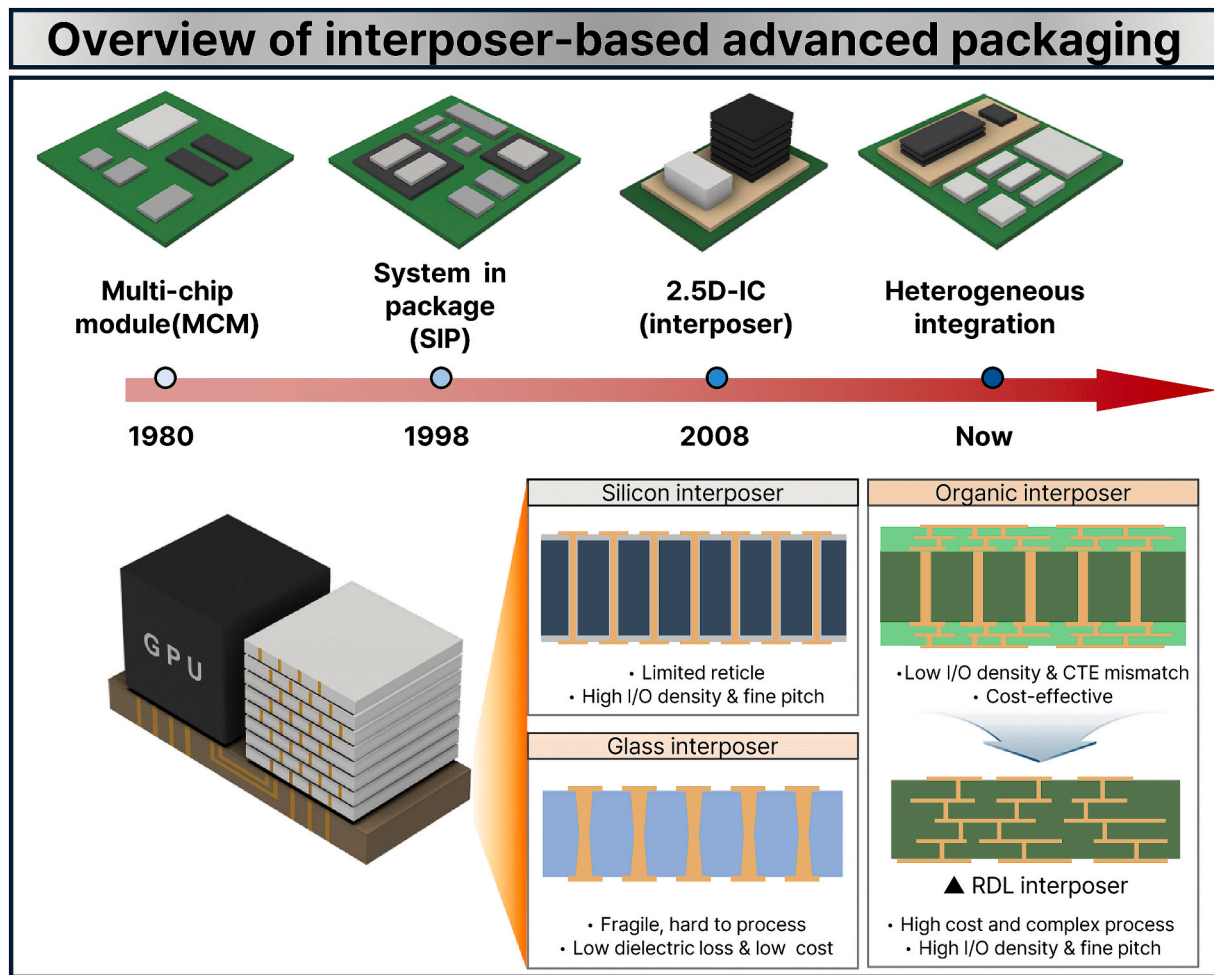


Fig. 1. Evolution of packaging toward interposer-based advanced packaging and platform comparison of silicon, glass, and organic interposers.

architecture is defined as a 2.3D IC integration. 2.5D IC integration refers to configurations in which multiple chips are supported by a passive through-silicon via (TSV) interposer and then attached to a package substrate. Finally, 3D IC integration is generally referred to as a packaging approach, in which multiple dies are integrated on an active TSV interposer and subsequently connected to a package substrate. Some studies have used the term 3D IC integration to describe single-die implementations on active TSV interposers [11]. With the evolution of these integration schemes, die-to-die interconnects require a higher input/output (I/O) density and finer routing pitch, underscoring the critical role of interposers in achieving the targeted performance. The progress of high-density packaging architecture also enables the chiplet-based heterogeneous integration of diverse functions, such as logic, memory, analog, and radio-frequency components, leading to simultaneous improvements in system performance, bandwidth, and power efficiency.

In heterogeneous integration packages, the term interposer is derived from the Latin phrase that means “to put between” and describes a structure positioned between dies to provide high-density routing and fine-pitch interconnects. When an interposer is paired with TSV-based vertical interconnects, it can provide higher routing density than conventional packaging substrates [12]. Hence, interposers have been explored as a fundamental technology for realizing high-bandwidth, low-latency, and low-power die-to-die connections. As illustrated in Fig. 1, interposers are generally divided into silicon, glass, and organic interposers based on their material platforms and design. Each has advantages and disadvantages related to electrical performance, thermo-mechanical characteristics, manufacturing cost, and process

Table 1

Comparison of interposer dimensions reported in the literature.

Interposer type	thickness [mm]	length [mm]	width [mm]	Ref.
Silicon	0.32	100	100	[15]
Silicon	0.3–0.5	–	–	[16]
Silicon	0.3	25	25	[17]
Silicon	0.5	10	–	[18]
Organic	0.4	–	–	[19]
Organic	0.2	15	14	[20]
Organic	–	2.5	2.5	[21]
Organic	0.4	38	30	[22]
Glass	0.2	25	25	[23]
Glass	0.13	–	–	[24]
Glass	0.1	–	–	[25]
Glass	0.5	16.5	13	[26]

complexity. Silicon interposers, the most established implementation, provide fine-pitch routing and high I/O density. However, they are associated with high manufacturing costs and high-frequency electrical limitations of lossy substrates [13,14]. Thus, research on glass and organic interposers has recently intensified to compensate for and complement Si interposers. In addition, RDL-based interposers that evolved from organic interposer technologies without relying on through-via have also been actively investigated as alternative platforms. However, the interposers listed in the literature differ substantially depending on their geometry, thickness, length, and width, and their design targets also differ depending on the field and process used, as described in detail in Table 1. This diversity is problematic when

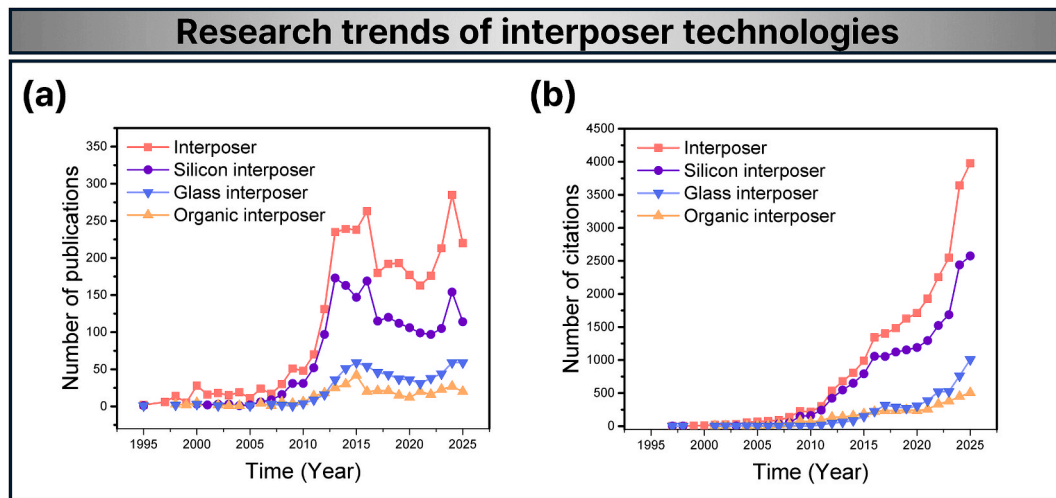


Fig. 2. Research trends in interposer technologies: (a) annual publications and (b) citations by interposer type. Publication and citation data were collected from the “Web of Science” database using the keywords “Interposer”, “Silicon interposer”, “Glass interposer”, and “Organic interposer”.

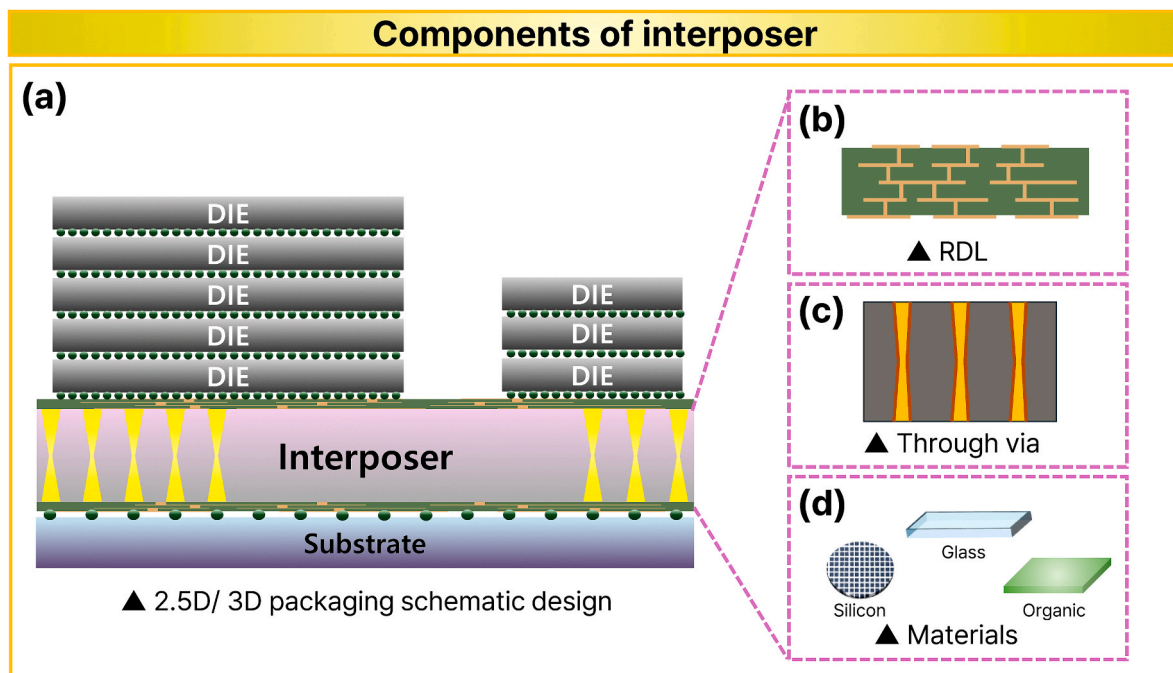


Fig. 3. Interposer architecture and constituent elements: (a) interposer-based multi-die integration, (b) multilayer RDL redistribution, (c) through-via vertical interconnection, and (d) typical interposer materials.

comparing and combining the merits, flaws, and research directions of a single-material platform. Thus, this study systematically analyzed the features specific to the material and related research trends of silicon, glass, and organic interposers. We expect that this comparative examination of how each technology enhances its strengths and addresses its limitations will guide application-driven interposer selection and future research. To address the inconsistent use of the term RDL in the literature, this review first distinguishes between base-material platforms and interconnect schemes, and then compares silicon, glass, organic/polymer, and hybrid interposer architectures.

A numerical representation of the research trends in interposer technologies is presented in Fig. 2(a) and 2(b), which describe the number of academic publications and citation counts, respectively. Fig. 2(a) demonstrates the steep trajectory of publications in the early 2010s and a temporary reduction around 2016. Since the early 2020s,

related research has begun to increase once more. Thus, we deduce that several factors, notably the spread of artificial intelligence accelerators, high-performance computing, and high-bandwidth memory (HBM)-based applications, along with increased attention to large-area interposers and reliability issues, have jointly contributed to this increase. Fig. 2(b) shows the general citation trends, indicating a persistent interest among academics in the interposer field. In this review, we compare the advantages and disadvantages of different interposer technologies in high-density packaging environments from the perspectives of electrical, thermal, and mechanical properties and reliability, and suggest an upcoming research direction based on the performance, cost, and reliability of next-generation semiconductor packaging.

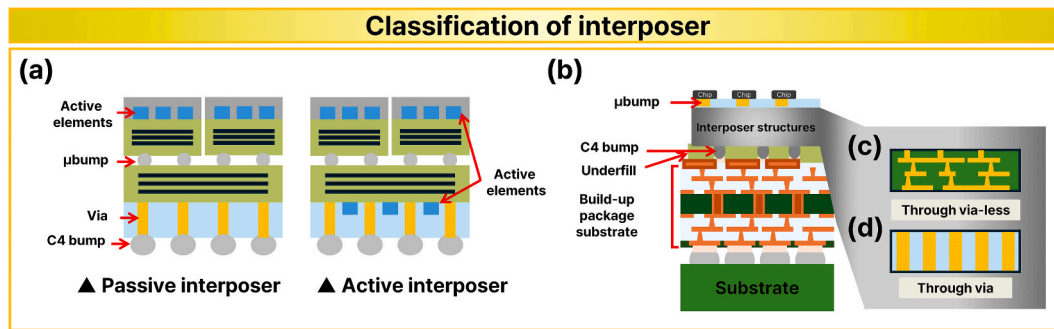


Fig. 4. Interposer architectures organized along two axes, base material and vertical-interconnect scheme: (a) silicon interposers in passive and active configurations, (b) organic/polymer interposers in a build-up configuration, (c) through-via-less, RDL-only interposers, and (d) through-via-based interposers (TSV/TGV). Panels (c) and (d) indicate interconnect schemes rather than separate base materials: the through-via-less, RDL-only configuration in (c) is most commonly realized on an organic/polymer platform and is referred to as an “RDL interposer.”.

2. Components and structure of interposer

To enable 2.5D and 3D integrated packaging, interposers serve as key building blocks that allow multiple ICs to be integrated heterogeneously within a single package. Interposers extend dense I/O interfaces to package-scale routing by providing ultra-fine-pitch wiring capability with line spacing below 1 μm , thereby supporting high-bandwidth chip-to-chip communication under stringent form-factor constraints [27–29]. In this context, the interposer configuration can be described as a combination of the (1) RDL, (2) through-via, and (3) supporting substrate material [30–32]. Fig. 3 illustrates the common structural architecture of interposers. As shown in Fig. 3(b), a multilayer RDL redistributes chip- or package-level inputs and outputs through lateral interconnections. As the routing density increases, this lateral redistribution becomes the primary enabler of a high I/O fan-out while maintaining a controlled signal and power distribution within the package [33,34]. The redistributed signals and power are then vertically connected through the interposer using through-via, as shown in Fig. 3(c), which directly links the upper and lower sides of the interposer. This short vertical path reduces the interconnect distance at the system level and can translate into a higher bandwidth and lower power consumption compared with longer lateral detours [35,36]. Because the RDL/through-via network must remain mechanically stable and electrically continuous throughout fabrication and operation, the substrate material becomes a governing design variable that simultaneously constrains the routing capability, reliability, and manufacturability. Fig. 3(d) shows the representative substrate materials used for the interposers, including silicon, glass, and organic materials [37–41]. Through the integration of these components, interposers are regarded as a suitable technology for packaging environments that require ultrahigh density and high performance [42,43].

Building on this distinction, this section classifies interposer architectures according to two independent criteria: the base substrate material and the vertical-interconnect scheme. Here, RDL (redistribution layer) refers to the fine-line metal/dielectric build-up used to laterally redistribute I/O. It is treated as a structural element rather than a base-material class. Accordingly, interposers are classified by base substrate material, including silicon, glass, and organic/polymer platforms, and by vertical-interconnect scheme, including through-via-based and through-via-less integration [11]. Under this convention, an “RDL interposer” indicates a through-via-less organic/polymer-based platform with multilayer RDL formed on a carrier. It is therefore regarded as a sub-type of the organic interposer family rather than a fourth independent material platform. Hybrid bridge-embedded architectures are discussed separately below.

In industry, silicon remains the most widely commercialized interposer material because its mature wafer infrastructure and fine-feature process compatibility provide a direct path to high-density RDL and

through-via integration at scale. Structurally, silicon interposers are classified into passive and active types, as shown in Fig. 4(a). A passive interposer represents a conventional approach in which the interposer serves solely as a connection substrate, incorporating only RDL and TSV. This architecture can interconnect chiplets. However, because signal conditioning must be handled outside the interposer, the limited on-interposer drive support makes it challenging to maintain robust signal integrity as the channel length and I/O density increase. Active interposers address this limitation by integrating transistor-based devices such as repeaters and clock buffers within the interposer, thereby expanding the design flexibility and improving the signal integrity (SI)/power integrity (PI) margins through localized buffering and distribution. However, this benefit is obtained at the expense of an increased interposer area and additional process steps, which can introduce yield risks and increase manufacturing costs [44,45].

Glass interposers have a different rationale. Because glass is electrically insulated, the integration of active devices within the substrate is less emphasized, and glass platforms have been predominantly studied as passive interposers that exploit routing- and via-based interconnections together with passive component integration. In particular, the low dielectric loss of glass provides a material-driven pathway for RF-oriented performance gain. By placing radio-frequency filters and resonators on the interposer, reported demonstrations have achieved low insertion losses, including filter insertion losses less than 1.8 dB [46]. Thus, glass does not merely replace silicon as a substrate but shifts the value proposition toward loss-limited applications, where the dielectric performance directly maps to measurable radio frequency metrics.

Organic interposers, as illustrated in Fig. 4(b), are enabled by a panel-manufacturable build-up concept. Rather than employing the through-via-based approach shown in Fig. 4(d), organic interposers adopt the through-via-less scheme illustrated in Fig. 4(c), stacking build-up layers on the substrate and forming interlayer connections using microvias. The key advantages are manufacturability and cost because panel-based semi-additive processes (SAP) can be leveraged for large-area production. However, as the routing density increases and scaling proceeds toward finer features, the same build-up strategy faces practical barriers, including limited scalability and inherent constraints associated with the coefficient of thermal expansion (CTE) and thermal conductivity of organic dielectrics [47,48]. These material- and process-driven limitations can manifest as warpage and integration challenges as the layer count increases, motivating alternative integration routes when the performance targets become more stringent.

This shift has contributed to the emergence of wafer-level RDL interposers, particularly when higher bandwidth and integration demands exceed what panel-based build-up flows can economically support. As higher bandwidth and integration are required, panel-based build-up processes have encountered challenges such as increased warpage with

Table 2

Comparison of thermo-mechanical and thermal property ranges for interposer substrate materials silicon, glass and organic materials [55–71].

Properties	Silicon	Glass	Organic(polymer)
Density [kg/m ³]	2329–2380	2203–2500	–
Young's modulus [GPa]	130–170	64–73	1.1–17
Poisson's ratio	0.2–0.3	0.16–0.23	0.2–0.3
CTE [ppm-K ⁻¹]	2.6–2.8	0.52–9.4	10–70
Thermal conductivity [W/(m-K)]	130–150	0.67–1.53	–
Specific heat capacity [J·kg ⁻¹ ·K ⁻¹]	700–750	703–840	–

layer count and high chemical-mechanical polishing (CMP)-related processing costs, which has accelerated interest in wafer-level RDL interposers. RDL interposers enhance performance and integration density by forming a multilayer SAP-based RDL on organic polymer dielectric layers [49,50]. Accordingly, interposer architectures are strongly influenced by the choice of substrate material, not only because the material dictates feasible process flows but also because it determines which bottlenecks dominate as design scales. Under this classification, wafer-level RDL interposers are therefore categorized as through-via-less variants of the organic/polymer platform rather than as a separate material class.

Beyond conventional silicon, glass, and organic/RDL platforms, hybrid bridge-embedded interposers have recently emerged as an intermediate architecture that addresses the density-cost-scalability trade-off of monolithic interposer platforms. In this approach, the full package area is not supported by a single large silicon interposer. Instead, small silicon bridges are embedded only in regions where high-density die-to-die routing is required, while the surrounding organic/RDL substrate provides the remaining signal and power distribution. Intel's embedded multi-die interconnect bridge (EMIB) is a representative example, in which a localized silicon bridge is embedded in an

organic package substrate to provide high-density and high-bandwidth chip-to-chip interconnection [51]. TSMC's (Taiwan Semiconductor Manufacturing Company) CoWoS-L (chip-on-wafer-on-substrate with a local silicon interconnect bridge) follows a related concept by combining local silicon interconnects with redistribution-layer routing, thereby retaining silicon-level local routing capability while reducing the reticle-size, cost, and yield constraints associated with full-area silicon interposers [52]. In this sense, bridge-embedded architectures should be interpreted as a hybrid interconnect strategy implemented on an organic/RDL platform rather than as a new base-material class.

This architecture has a direct design implication. Because fine-pitch interconnects are concentrated only in the bridge region, high-bandwidth chiplet-to-chiplet communication can be supported without extending silicon-class routing across the entire package area. Recent silicon-bridge test vehicles based on the Universal Chiplet Interconnect Express (UCIe) specification further show that bridge-based routing can support high-speed die-to-die links when bump pitch, bridge layout, and channel design are jointly optimized [53]. However, the same localization strategy introduces additional process and reliability bottlenecks. The silicon-bridge/organic interface can concentrate coefficient-of-thermal-expansion (CTE) mismatch, while cavity formation, bridge placement, bump-height uniformity, and build-up thickness variation can affect interfacial adhesion and assembly yield [54]. Therefore, bridge-embedded interposers should be regarded as a coupled material-process-layout solution in which chiplet placement, bridge layout, routing density, and thermo-mechanical reliability must be co-optimized [69].

These material-dependent bottlenecks become clearer when the thermo-mechanical properties are interpreted as drivers of deformation, stress evolution, and heat-spreading behavior rather than as standalone numbers, as summarized in Table 2. For silicon, representative property ranges commonly used in the literature include a density of 2329–2380 kg/m³, Young's modulus of 130–170 GPa, Poisson's ratio of 0.20–0.30, CTE of 2.6–2.8 ppm/K, thermal conductivity of 130–150 W/m-K, and specific heat capacity of 700–750 J/kg-K [55–62]. The combination of high stiffness and low CTE generally stabilizes global deformation under

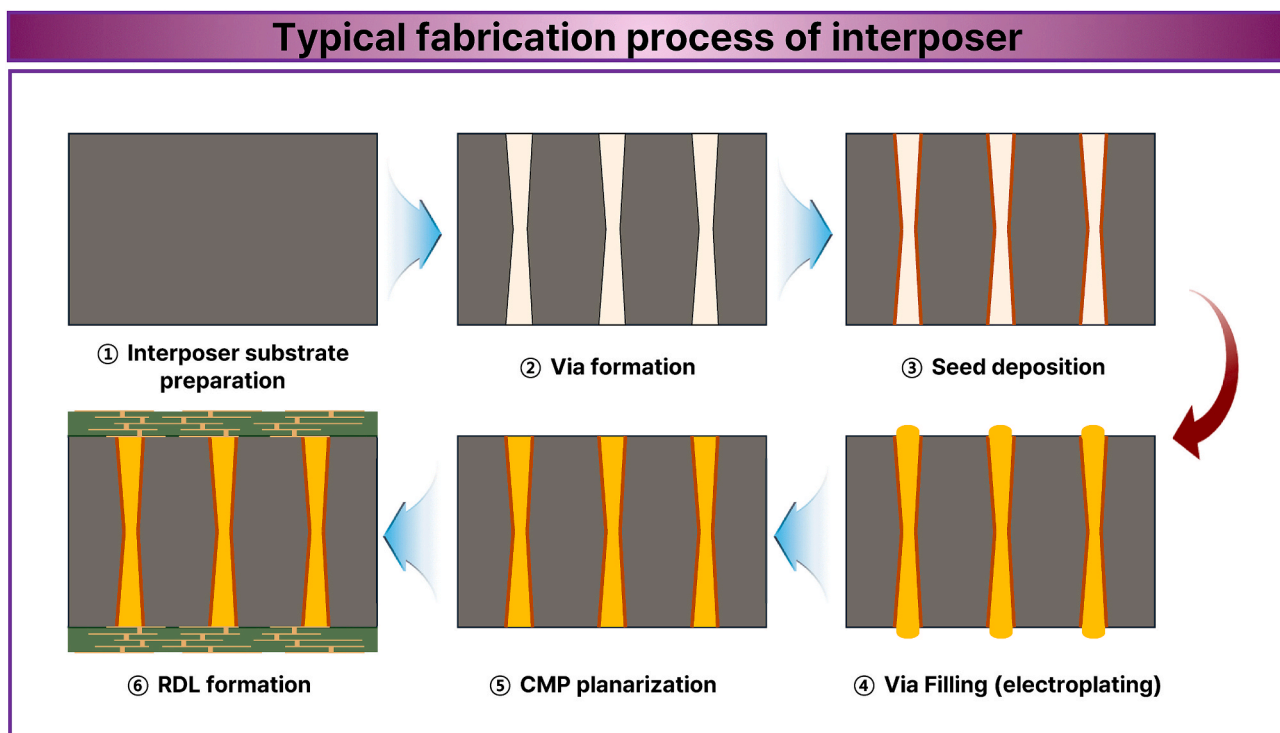


Fig. 5. Schematic of a typical interposer fabrication process.

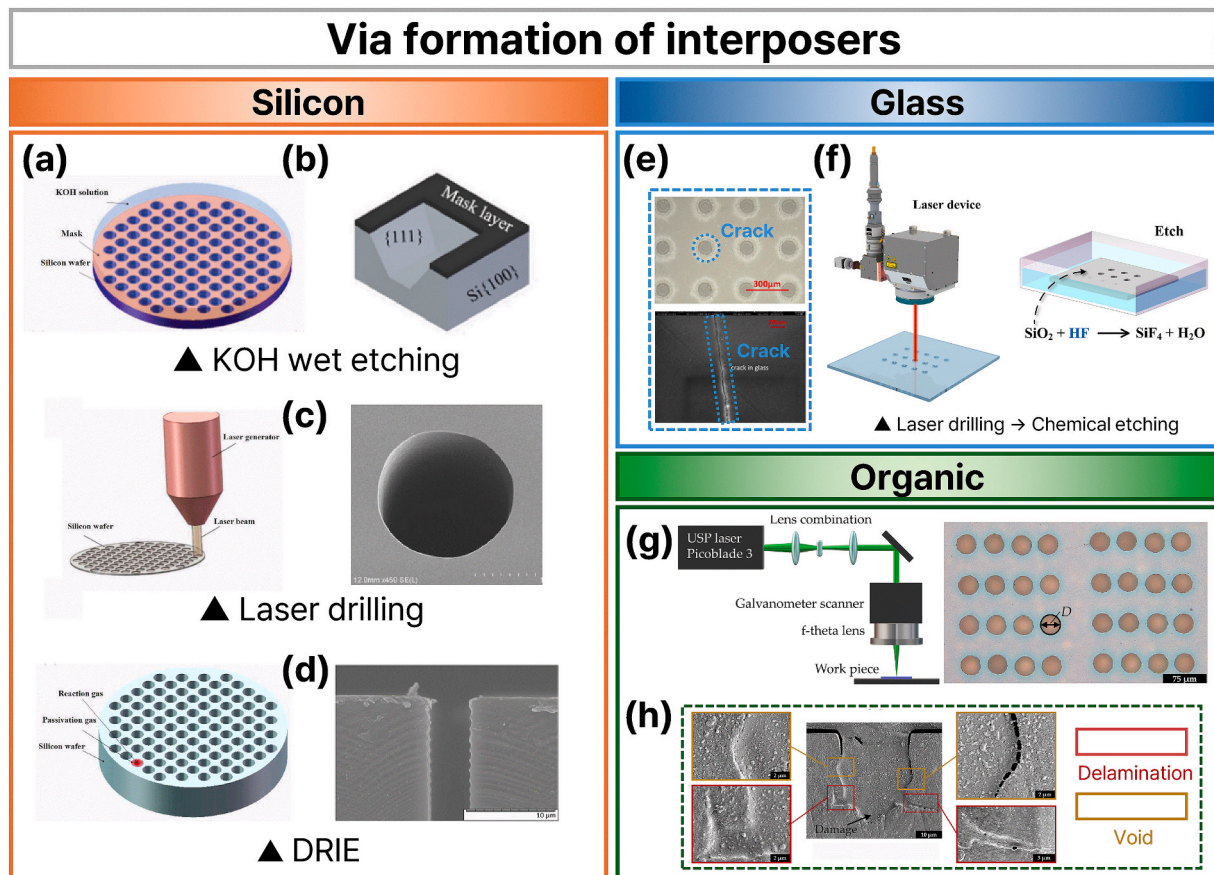


Fig. 6. Schematic of via formation in interposers: (a) representative via formation techniques in silicon interposers, including KOH-based wet etching, laser drilling, and DRIE. Adapted from [73], (b) crystallographic orientation-dependent via geometry produced by anisotropic KOH wet etching. Adapted from [74] under the terms of the Creative Commons CC BY license, (c) typical via morphology formed by laser drilling in silicon substrates adapted from [76], (d) via profiles fabricated by DRIE in silicon interposers. Adapted from [77] under the terms of the Creative Commons CC BY license, (e) laser-induced microcracks and damage observed in glass substrates after via drilling. Adapted from [81], (f) combined laser drilling and chemical etching process for via formation in glass interposers. Adapted from [80], (g) ultrashort-pulse laser drilling system and resulting micro-via array in organic substrates. Adapted from [83] under the terms of the Creative Commons CC BY license, (h) interfacial defects such as delamination and voids formed during laser-drilled micro-via fabrication in organic interposers. Adapted from [83] under the terms of the Creative Commons CC BY license.

thermal loading, which is beneficial for alignment and structural stability. However, because silicon is significantly stiffer than many surrounding package materials, a stiffness mismatch can concentrate interfacial stresses, increasing the likelihood that interfaces, rather than the silicon itself, become reliability-critical locations.

Glass interposers occupy an intermediate position. They exhibit densities of 2203–2500 kg/m³, Young's moduli of 64–73 GPa, Poisson's ratios of 0.16–0.23, and composition-dependent CTEs spanning a wide range of 0.52–9.4 ppm/K, enabling CTE tailoring as a design variable. However, their thermal conductivity of 0.67–1.53 W/m·K and specific heat capacity of 703–840 J/kg·K [63–66] are substantially lower than those of silicon, which implies that heat spreading through the substrate is limited and thermal pathway design must be explicitly addressed to avoid heat localization. Nevertheless, because glass offers an intermediate stiffness between silicon and organic substrates, together with high CTE design flexibility, it can serve as an effective option for deformation and stress management when the package is designed as a coupled system rather than as a single-material substrate.

Organic interposer employs polymer dielectric-based build-up structures, such as ajinomoto build up film (ABF), with typical properties including a Young's modulus of 1.1–17 GPa, Poisson's ratio of 0.20–0.30, and a CTE of 10–70 ppm/K [67–71]. Here, the low stiffness and high CTE imply that thermal loading is more readily converted into global warpage and time-dependent deformation, which can amplify the stress at metal-polymer interfaces and accelerate failure modes such as

lifetime degradation and interfacial delamination. In other words, the same material attributes that enable a manufacturable build-up architecture can introduce thermo-mechanical penalties that directly constrain the fine routing stability and long-term reliability.

In conclusion, interposer materials present distinct design constraints and trade-offs depending on their thermo-mechanical properties and process characteristics. Because optimal material and architecture vary with the application requirements and target performance, application-driven material selection and structural optimization are essential.

3. Interposer fabrication

To understand the physical differences between the interposer platforms presented in Fig. 5, it is useful to begin with a common fabrication framework. Typically, interposer fabrication proceeds through via formation, liner/seed formation, metal filling, planarization, and RDL formation after substrate preparation [72]. Although this sequence is broadly shared across materials, each platform exhibits material-specific process constraints that translate into distinct defect modes, and consequently, different electrical, thermal, and reliability outcomes. In this section, we compare how the process implementation diverges for each material and how these differences propagate to performance-limiting bottlenecks.

Table 3

Summary of via-formation methods for silicon, glass, and organic interposers, with typical via geometry and aspect ratio, advantages, and characteristic limitations and defects.

Method	Material	Profile / AR	Advantages	Limitations	Ref.
KOH wet etch	Silicon	Tapered ~ 54.7°, low AR	Simple, low cost	Fixed geometry, low AR	[73,87]
DRIE (Bosch)	Silicon	Near-vertical, AR > 10:1	Fine-pitch, high AR	Scalloping, slow, costly	[73,88]
Laser drilling	Si / glass / organic	Variable taper, maskless	Fast, large-area, flexible	HAZ/recast, microcracks, delamination	[71,73,82,89,90]
Laser + wet etch (LIDE/SLE)	Glass	Smooth taper, AR > 10:1	Crack-free high-AR vias	Narrow window, HF handling	[82,84,89,91]
Wet (HF) / sandblast / ECDCM	Glass	Conical, low AR (1–5)	Simple, low cost, fast	Low AR, rough, thermal damage	[82,89,91]
Dry plasma (ICP-RIE)	Glass	Moderate-vertical sidewalls	Litho-defined, batch	Very slow, mask erosion, costly	[82,85,89]
Photosensitive glass	Glass	High AR (>10), arbitrary shapes	Batch, arbitrary geometry	Special costly glass, multi-step	[82,85,89]
Laser microvia (CO ₂ /UV/excimer)	Organic	Tapered blind microvia	High throughput, small vias	Smear/taper, delamination	[71,92]
Photo-via (PID)	Organic	Fine parallel microvia	Batch, fine-pitch	Photo-definable only, loss trade-off	[71,89]
Mechanical drilling	Organic (core)	Large through-via	Low cost, high throughput	Coarse pitch, smear	[71,89]
Plasma (dry) via etch	Organic (flex)	Tapered ~ 45–70° microvia	Batch, residue-free fine vias	Less mature, masking needed	[71,86,92]

3.1. Via formation

Via formation is not merely a via-making step. It defines the initial defect population and geometric boundary conditions that govern the subsequent metallization continuity and filling stability, thereby shaping the final electrical path quality and reliability margin. Fig. 6 shows that the dominant via formation method varies by material platform, and that each method tends to introduce characteristic geometries and defect patterns that later appear as measurable performance degradation.

Fig. 6(a) shows the major via-formation routes for silicon interposers, where KOH wet etching, laser drilling, and deep reactive ion etching (DRIE) are selected according to the process objectives [73]. In KOH-based wet etching, Fig. 6(b) shows a strong dependence on the crystallographic orientation [74]. Because anisotropic etch rates naturally produce tapered sidewalls and facet geometries at fixed angles, this method provides process simplicity but limits geometric freedom [75]. This geometric constraint is not only a layout concern. This directly constrains achievable via profile and routing density, which can restrict the aggressive scaling of vertical interconnects for electrical performance targets. Fig. 6(c) shows the vias formed by laser drilling in silicon. The high speed and flexibility of laser processing make it attractive for large-area implementation. However, thermal effects must be controlled [76]. If the heat-affected zone and recast layer are not adequately managed, subsequent seed formation and plating can become locally nonuniform, increasing the probability of discontinuities that manifest resistance dispersion and loss variation along high-speed channels. Fig. 6(d) shows DRIE profiles on silicon [77]. DRIE enables fine-pitch and high-aspect-ratio features with good verticality, which is advantageous for dense interposer routing. However, sidewall roughness and microdamage can persist depending on the process conditions, requiring post-treatments to avoid the propagation of these defects into the metallization step [78]. In practice, residual roughness or damage can translate into nonideal metal coverage and weak interface points, which later contribute to increased loss and reliability degradation under thermal and electrical loading.

The material nature of glass interposers makes the implementation of high-speed, high-precision plasma dry etching challenging, which is comparable to that of silicon. Amorphous SiO₂-based glass imposes significant burdens on plasma dry etching in terms of etch rate, uniformity, and cost, and achieving a high throughput for thick substrates is challenging [79]. Thus, via formation commonly relies on laser-based processing followed by chemical etching to adjust the taper and remove the damaged layers, as illustrated in Fig. 6(f) [80]. This combined route has significant performance implications. As shown in Fig. 6(e), laser drilling can introduce microcracks and damaged layers [81], which are mechanically critical features of a brittle substrate. Chemical

etching can remove portions of the damaged layer and tune the taper. However, when the process window is narrow, residual defects or shape deviations may persist. Because glass is intrinsically brittle, residual initial cracks can act as stress concentrators and promote defect growth during subsequent processing and thermal excursions, thereby increasing the likelihood of reliability issues [82]. Thus, in glass platforms, via formation quality directly determines the risk level for later interfacial delamination/cracking, which ultimately constrains the allowable thermal cycling and long-term package stability.

Organic interposers are structurally centered on core-build-up laminations and microvias, rather than through-via. As shown in Fig. 6(g), via formation is largely based on laser drilling. However, polymer dielectrics are sensitive to heat input and decomposition behavior. Consequently, Fig. 6(h) shows that interlayer delamination or voids can occur, depending on the process conditions. However, these are not merely visual defects. They can drive practical electrical and reliability penalties by degrading seed-layer continuity, inducing nonuniform filling, and weakening interfacial adhesion, which collectively reduces long-term reliability [83].

Therefore, across glass and organic platforms, via defects not only reduce the yield and reliability, but also hinder stable metallization and uniform filling in the subsequent steps. Controlling via geometry and damage is a prerequisite for stable metal formation because the “starting condition” of the surface and interface largely determines whether metallization yields a continuous, low-loss conductive pathway or a defect-prone interconnect network.

Because via formation establishes the geometric and defect “starting condition” for all subsequent metallization, the appropriate technique differs markedly across the three platforms, and several distinct routes coexist within each material. Table 3 consolidates these routes and maps each method to its applicable material, typical via geometry and aspect ratio, advantages, and characteristic limitations. For silicon, via formation benefits from a mature etching toolbox: anisotropic KOH wet etching is simple and low-cost but yields orientation-fixed tapered profiles with limited aspect ratio, whereas deep reactive-ion etching (DRIE, Bosch process) delivers near-vertical, high-aspect-ratio vias suited to dense routing at the expense of sidewall scalloping and higher cost. Wet electrochemical etching offers a lower-cost, high-aspect-ratio alternative [73], and laser drilling adds a fast, maskless route for large-area or via-last schemes, provided the heat-affected zone and recast layer are controlled.

Glass exhibits the widest method diversity, precisely because no single route is dominant. Direct laser ablation is fast but tends to seed microcracks in the brittle substrate, so it is often combined with a subsequent chemical etch: laser modification followed by selective wet etching (laser-induced deep etching/selective laser etching, LIDE/SLE) removes the damaged layer and produces crack-free, high-aspect-ratio

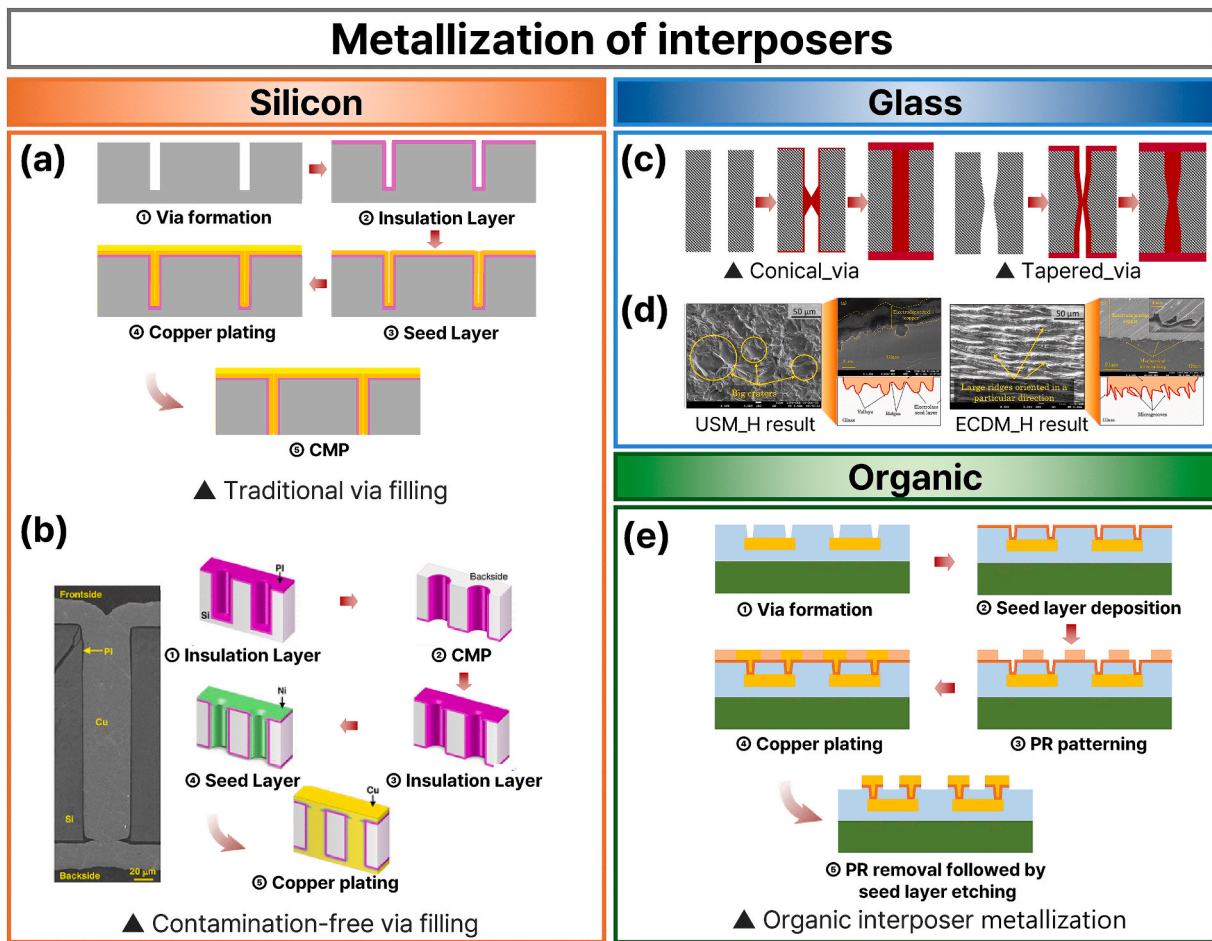


Fig. 7. Representative metallization process flows for silicon, glass, and organic interposers, highlighting the dominant bottlenecks governing electrical continuity and thermo-mechanical reliability: (a) conventional TSV metallization flow in silicon interposers: liner/barrier-seed deposition, Cu electroplating, and CMP planarization, (b) process modification for improved electrical stability in silicon TSV using a double-sided flow with a polyimide-nickel functional layer. Adapted from Ref. [97] under the terms of the Creative Commons CC BY license, (c) effect of TGV geometry on metallization/plating behavior in glass interposers. Adapted from Ref. [112], (d) surface conditioning/roughening approaches to enhance metal-glass interfacial adhesion and stabilize metallization. Adapted from Ref. [113], (e) typical semi-additive (SAP/MSAP) metallization flow for organic interposers: ① microvia formation, ② seed-layer deposition, ③ PR patterning, ④ Cu pattern electroplating, and ⑤ PR removal followed by seed-layer (flash) etching, which electrically isolates the redistribution lines. Adapted from Ref. [71,92] under the terms of the Creative Commons CC BY license.

vias with tunable taper [84]. Isotropic wet (HF) etching, sandblasting, and electrochemical-discharge machining (ECDM) are equipment-simple but limited in aspect ratio and surface quality, while inductively coupled plasma reactive-ion etching (ICP-RIE) gives lithographically defined vias at very low etch rates [85], and photosensitive (photostructurable) glasses such as Foturan and APEX enable parallel, arbitrarily shaped high-aspect-ratio vias at the cost of specialized, expensive glass and multi-step processing [85]. Organic substrates, being build-up-based, rely chiefly on laser-drilled microvias (CO₂, UV, or excimer) and photo-vias patterned in photo-imageable dielectrics for fine interlayer connections [67], with mechanical drilling reserved for larger plated through-holes in the core layer and plasma (dry) etching offering a parallel, residue-free route for fine vias in non-photosensitive polymers, particularly on flexible substrates [86]. Across all platforms the practical choice balances achievable aspect ratio, throughput, induced damage, and cost. Because residual cracks, recast, or delamination introduced at this stage propagate into seed-layer discontinuities and plating defects, via-formation quality ultimately bounds the attainable metallization continuity and long-term reliability. As a practical selection guide, DRIE is preferred where high-aspect-ratio, vertical silicon vias are required, whereas laser modification plus chemical etching (LIDE/SLE) is favored for crack-free, high-aspect-ratio

glass vias. Photosensitive glass and ICP-RIE suit batch, lithographically defined glass vias and laser-drilled microvias (UV/excimer) or photo-vias dominate fine organic interlayer connections, with mechanical drilling reserved for large core through-holes.

3.2. Metallization

The taper, sidewall roughness, and damage layer defined during via formation directly influence the difficulty and outcome of metallization [93]. Metallization aims to establish a continuous conductive path along the via sidewalls and bottom, enable stable void-free filling via electroplating, and provide a planar surface for subsequent wire formation [94,95]. In practice, these goals directly map electrical resistance/loss stability, high-frequency integrity, and thermo-mechanical reliability. The dominant bottleneck differs according to the material platform, as shown in Fig. 7.

For silicon interposers, Fig. 7(a) shows the conventional flow in which an insulating liner and barrier/seed layers are deposited after via formation, in which the vias are filled through Cu electroplating, and the overburden is removed by CMP. Under this flow, void-free copper filling becomes the primary determinant of both reliability and electrical performance [96]. The reason for this is clear. Any seam/void not only

Table 4

Quantitative comparison of achievable redistribution-layer line and space (L/S) resolution across silicon, glass, and organic interposer platforms, with the dominant enabling process and principal scaling limiter for each.

Platform	Typical L/S (HVM)	Best demonstrated L/S	Key enabler	Key limiter	Ref.
Silicon	~1–2 μm	~0.5 μm (BEOL Cu), sub- μm on roadmap	BEOL Cu damascene, wafer litho, CMP	Wafer/reticle cost, poor panel scaling	[71,124]
Glass	~2–10 μm	~2 μm (panel SAP), ~1 μm (research)	Fine litho, panel-scale SAP	Metal–glass adhesion, cracking	[89,125]
Organic	≥ 10 μm	~2 μm (advanced SAP)	Advanced SAP	Seed-etch undercut, warpage	[48,92,126]

increases the DC resistance but also disturbs the high-frequency current distribution and local heating, thereby amplifying signal loss and accelerating thermo-mechanical degradation during operation. To enhance the electrical performance within the silicon TSV framework, Fig. 7(b) illustrates a TSV technology that reduces the leakage current via a double-sided process incorporating a polyimide-nickel functional layer [97]. Here, the process modification targets an electrical bottleneck (substrate coupling/leakage), and the benefit appears to be improved electrical stability rather than a purely geometric improvement. From the viewpoint of filling integrity, high-aspect-ratio TSV are particularly prone to seams and voids owing to their nonuniform ion transport and additive distribution within the electrolyte. These defects lead not only to increased electrical resistance but also to long-term reliability degradation, including high-frequency signal loss and thermally induced stress [98]. To mitigate this problem, filling strategies have evolved from simple current control [99] to pulse/pulse reverse plating (PPR) and ultrasonic-assisted electroplating [100,101]. More recent efforts have shifted toward chemical control, including single-inhibitor bottom-up filling [102–104] and optimized combinations of levers and additives, to broaden the high-aspect-ratio process window [105–108]. In addition, because seed continuity is necessary for successful filling, electroless-based seed enhancement has been investigated to improve seed uniformity and reduce filling failures [109]. Collectively, these advances demonstrate a clear chain. Transport/additive nonuniformity induces void/seam formation, which then emerges as electrical loss/reliability penalties. Therefore, both electrochemical kinetics and seed continuity become design constraints for high-aspect-ratio TSV metallization.

The metallization of glass interposers differs fundamentally because glass is an insulator. Therefore, it does not require an insulating liner [110]. However, the absence of a liner does not eliminate this key bottleneck. Instead, the practical bottleneck is concentrated on metal-glass interfacial adhesion and seed-layer formation [89]. Glass surfaces are inherently smooth, and the substrate is brittle. Therefore, the residual microcracks from via formation or weak interfacial adhesion can readily evolve into delamination or cracking under thermal cycling [111]. This directly links the metallization quality to the thermo-mechanical reliability limits of glass packages. Fig. 7(c) shows the plating behavior as a function of through glass via (TGV) geometry [112], highlighting that the geometry still affects transport and coverage. However, as illustrated in Fig. 7(d), glass metallization generally prioritizes strengthening the mechanical interlocking through surface roughening or plasma activation [113]. This is because improved mechanical anchoring increases the effective interfacial toughness, which suppresses delamination initiation and stabilizes electrical continuity during thermal excursions. In addition, in high-aspect-ratio TGV, sputter-based seeds have limited depth wise uniformity [114], which can translate into discontinuous plating initiation and nonuniform filling. Consequently, recent studies have focused on securing continuous seed layers throughout the via interior through Pd-based activation, Pd-free seed processes, and hybrid seed formation schemes [115–119]. These efforts explicitly treat seed continuity as a bridge between process feasibility and electrical/long-term stability because discontinuous seeds appear downstream as plating defects, resistance scatter, and reliability risks.

For organic interposers, the emphasis of metallization shifts from merely filling deep vias to ensuring stable interlayer electrical continuity

within a core build-up stack [71,120–123]. As shown in Fig. 7(e), the aim of metallization is reliably to connect the microvias and RDL, rather than to achieve through-via filling. A typical process flow forms a seed layer through desmearing/cleaning, surface conditioning, PR patterning, Cu electroplating, and PR removal. The exposed seed layer is then removed by a flash (differential) etch to electrically isolate adjacent redistribution lines. Because this seed-layer etch is largely isotropic and its rate depends on local pattern density, it simultaneously recesses the conductor sidewalls and becomes a critical linewidth (CD)-controlling step at fine line/space. For example, recent 2/2 μm L/S RDL data show the plated line width changing from ~2.7 μm before seed etch to ~2.0 μm after etch [92]. In practice, because wet flash etching attacks the conductor isotropically, it produces sidewall undercut and lateral loss of the plated copper, so suppressing seed-etch undercut and CD loss becomes critical as organic RDL scales toward ~2 μm L/S [48,92]. Seed-layer etching is thus an integral, performance-determining step of the standard semi-additive or modified semi-additive process (SAP/MSAP) flow rather than a trivial closing operation [71]. Delamination or voids generated during surface preparation and conditioning readily lead to seed discontinuities and plating defects. Hence, contamination control is emphasized in organic interposer packaging. In organic and wafer-level RDL (WLRDL) interposers, metallization is characterized by the repeated requirement to secure seed continuity and interfacial reliability in fine-pitch patterns rather than by a single “deep via fill” event, which has direct design implications. Because the line and space dimensions decrease and the layer counts increase, even small variations in the surface conditions or residues can accumulate into systematic yield loss and reliability degradation through repeated interfacial weak points.

To make this platform comparison quantitative, Table 4 summarizes the achievable redistribution-layer (RDL) line/space (L/S) resolution for the three interposer families, together with the dominant enabling process and the principal scaling limiter of each. Silicon interposers, fabricated with back-end-of-line (BEOL)-class Cu damascene and high-resolution wafer lithography, currently provide the finest RDL L/S in the ~0.5–2 μm range, with sub- μm wiring on the roadmap [71], but at wafer-level cost and with limited panel scalability, and with via-level reliability such as electromigration in TSV and through-dielectric via (TDV) structures as a further design constraint [124]. Glass interposers occupy an intermediate position: their high dimensional stability, low CTE, and superior flatness allow semi-additive RDL to reach ~2 μm L/S at the panel scale (~1 μm reported in research) [89], provided that metal–glass adhesion, substrate handling, and RDL-induced cracking are controlled [89,125]. Organic interposers, historically limited to ≥ 10 μm L/S (a range that still represents roughly 70 % of high-volume-manufactured RDL), have advanced rapidly through advanced semi-additive processing, with high-density organic RDL reproducibly patterned down to 2/2 μm L/S in a fan-out flow [48,92]. This progression shows that, across all three platforms, sub-2 μm scaling is increasingly governed not by lithography alone but by seed-layer etching fidelity (undercut and CD loss) [92,126], warpage and CTE mismatch of the build-up/substrate stack [127], and interfacial adhesion, including RDL-induced cracking of the brittle glass substrate at higher layer counts [125], rather than by patterning resolution itself. In other words, the practical L/S limit on non-silicon platforms is set by metallization and thermo-mechanical integrity rather than lithographic capability, which is why advanced semi-additive processing and tight process-window control dominate the most recent glass and organic demonstrations.

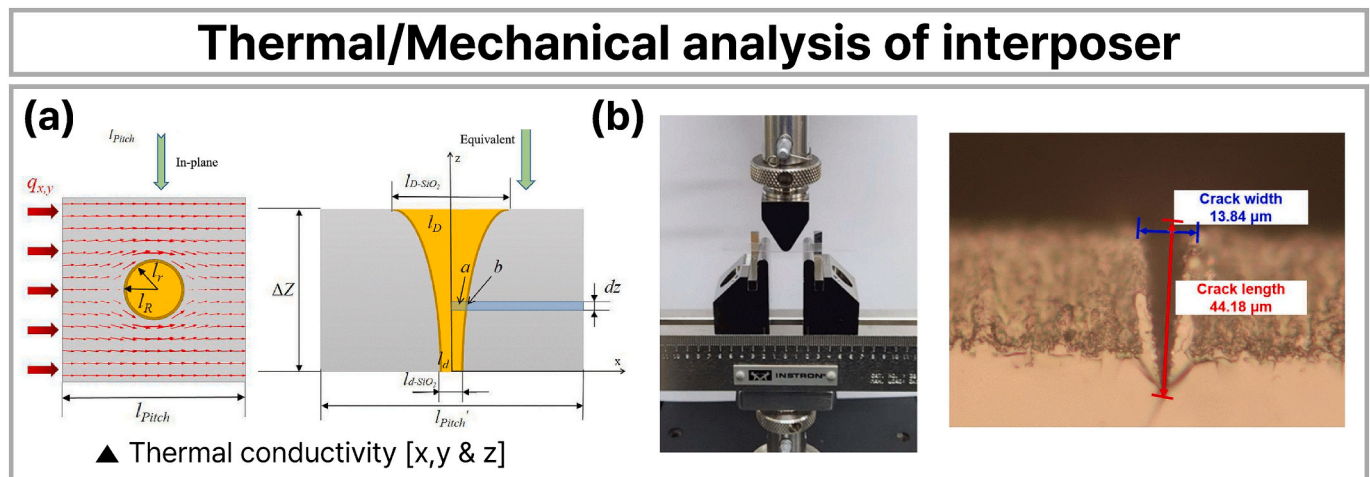


Fig. 8. Effective thermal and mechanical properties of interposers governed by embedded metal networks and brittle damage behavior: (a) schematic illustration of anisotropic effective thermal conductivity in interposers (in-plane versus cross-plane). Adapted from [130], highlighting the role of metal routing via networks in defining heat-flow paths, (b) representative mechanical reliability evaluation for brittle interposer substrates, illustrating damage/crack characterization under mechanical loading. Adapted from [147].

Finally, across all platforms, metallization must be interpreted not only as an electrically enabling step but also as a thermo-mechanical driver. Although metallization is critical for signal transmission, the Cu/liner/seed stacks formed during this process can alter the interfacial shear stress and package warpage depending on the thickness, processing temperature, and residual stress, thereby serving as initiation sites for microcrack propagation and delamination [34,128]. In other words, metallization simultaneously determines the electrical path quality and stress/warpage state that govern long-term package reliability, making process integration a coupled electrical-thermal-mechanical optimization problem rather than a purely conductive-path formation step.

4. Thermo-mechanical properties and reliability

In the previous section, interposer material platforms and their process implementations were compared. These structural and process choices should be viewed not only as determinants of manufacturing complexity and cost but also as factors that shape the dominant heat-flow paths and the effective stiffness of the interposer stack. Thus, they strongly influence the accumulation of warpage and the locations where stress is concentrated under real process thermal histories and operating temperature fluctuations, consequently setting the conditions under which damage initiates and electrical stability degrades in packaged systems.

4.1. Thermal and mechanical properties

In the 2.5D/3D packages, the interposer is positioned directly beneath the high-power logic and HBM. Therefore, its architecture simultaneously governs in-plane heat spreading and cross-plane heat removal [129]. Under this role, the “effective” thermal behavior is rarely dictated by the substrate material alone because the metal network embedded in the interposer provides preferential heat-flow paths. Fig. 8 (a) illustrates this point by showing that metal routing can directly modify the effective thermal conductivity beyond that expected from the intrinsic material properties alone [130].

For silicon interposers, the base substrate provides relatively high thermal conductivity and near-isotropic heat conduction. However, TSV insertion transforms the interposer into a repeated composite of Si-liner/insulator-Cu, rather than monolithic bulk Si [131,132]. This structural change produces clear pathway-level consequences. Cross-plane heat transport is dominated by continuous Cu-filled TSV pathways, whereas

in-plane heat spreading is increasingly governed by the distribution and areal fraction of planar metals and the RDL [133,134]. Thus, TSV insertion does not necessarily translate into uniform “thermal improvement.” Instead, it can strengthen thermal anisotropy as a function of the metal volume fraction and spatial arrangement, which becomes a design constraint when thermal gradients must be minimized under localized hotspots [135,136].

This mechanism is more pronounced in glass interposers because the substrate itself has a low thermal conductivity, which suppresses heat diffusion through the bulk glass and increases the fraction of heat that must be carried by the TGV metal fills and RDL/planar metal layers [137,138]. Consequently, the effective thermal conductivity of the glass interposers cannot be determined using a simple material-averaged value. The cross-plane transport is strongly governed by the TGV array, whereas the in-plane spreading is primarily determined by the routing density and metal layout [139]. In other words, the thermal performance of glass-based platforms becomes a routing and via-architecture problem rather than a substrate-property problem, indicating that the thermal design must be co-optimized with electrical routing decisions.

Similar coupling appears in organic and WLRDL interposers. Because these platforms rely on stacked polymer dielectrics, heat transport becomes strongly dependent on the embedded copper network [140,141]. Considering the low thermal conductivity of polymers, cross-plane heat transport is prone to bottlenecks imposed by dielectric layers and limited vertical connections, whereas in-plane spreading varies significantly with the metal pattern density and routing orientation [142]. Therefore, for polymer-based platforms, routing choices simultaneously affect the feasibility of SI/PI routing and the in-plane thermal spreading capacity, linking the electrical density targets to thermal constraints.

From a mechanical perspective, the same structural motifs that shape the thermal pathways also determine stiffness and defect sensitivity. Silicon and glass exhibit high stiffness owing to their high elastic moduli and hardness. However, their brittle nature makes them more defect-sensitive [143,144]. In glass, microdamage introduced during via formation, such as cracks or chipping, can sharply reduce strength [145,146]. Fig. 8(b) illustrates an evaluation approach for brittleness-driven damage behavior [147]. In contrast, organic/polymer-based materials are more compliant, and their mechanical responses often evolve over time and temperature rather than remaining constant [148–151]. This time/temperature dependence implies that mechanical loading can be redistributed during thermal excursions, making warpage and interfacial damage sensitive to both thermal history and

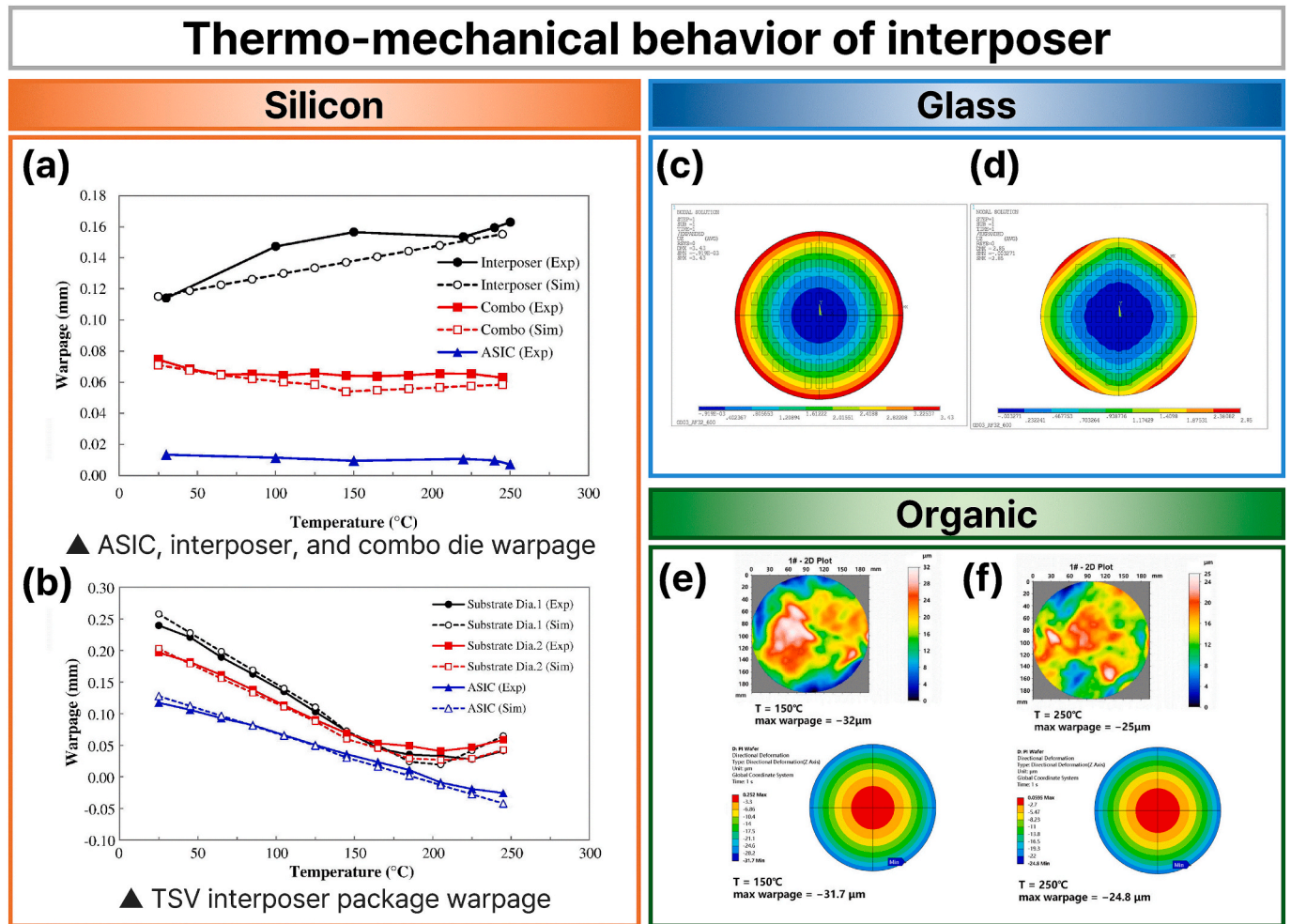


Fig. 9. Material-dependent warpage behaviors of silicon, glass, and organic/WLRDL interposer packages. Silicon TSV package warpage: (a) constituent-level warpage versus temperature, (b) package-level warpage versus temperature. Adapted from [159], glass-interposer package warpage distribution: (c) case 1, (d) case 2. Adapted from [162], and organic package warpage-field: (e) 150 °C, (f) 250 °C. Adapted from [167] under the terms of the Creative Commons CC BY license.

dwell time.

In summary, the interposer heat transport and stiffness are best described as equivalent properties emerging from the combined effects of vias, routing, and layer stacking, rather than as intrinsic substrate properties alone. These equivalent properties manifest as global warpage and localized stress concentrations under processing and operating thermal loads, with the dominant governing factors varying across interposer systems.

4.2. Thermo-mechanical behavior

The thermal pathways and effective stiffness discussed above are observed in practice as coupled warpage evolution and localized stress concentrations under process thermal histories and operating temperature fluctuations [152,153]. In 2.5D/3D stacks, this coupling is amplified because the interposer is located directly beneath the high-power dies and forms a heterogeneous composite in which multilayer routing, vias, and underfill are superimposed, making the thermal and mechanical requirements prone to conflict within the same structure [154,155]. Under these conditions, warpage should not be treated as a simple geometric deformation. Rather, it originates from the superposition of the CTE mismatch, residual stress, stacking asymmetry, and package-level constraints such as stiffeners, molding compounds, and fixtures. Accordingly, the dominant contributors to the warpage shift depend on the interposer platform and stack configuration [156,157].

In silicon TSV-based interposers, die-to-interposer CTE matching is relatively favorable. However, warpage behavior cannot be explained solely by a single material-pair match [158]. Fig. 9(a) shows that even within silicon-based stacks, the temperature-dependent warpage differs according to the constituent components. Although an application-specific integrated circuit (ASIC) may exhibit relatively gradual deformation over a certain temperature range, the interposer can retain substantial residual warpage at room temperature and continue to accumulate out-of-plane deformation as the temperature increases [159]. This is because a silicon interposer is a multilayer composite stack incorporating TSV, inter-metal dielectrics, and passivation rather than bulk Si. Thus, process-induced residual stresses and stacking asymmetry can be amplified, particularly as the interposer becomes thinner [160]. The implication is that the process integration choices that determine the residual stress become part of the warpage design space, and not merely a fabrication detail. Moreover, the warpage reduction after ASIC-interposer stacking can be interpreted as a constraint-induced redistribution of the equivalent stiffness and neutral plane caused by the micro-bump and underfill layers, partially restricting the free deformation of the interposer. Consistent with this view, Fig. 9(b) shows that package-level warpage can follow different curves depending on the substrate geometry and reinforcement structures and can even undergo deformation-mode transitions over specific temperature ranges, emphasizing that warpage in silicon interposer packaging is governed by constraint conditions and stack architecture rather than by the

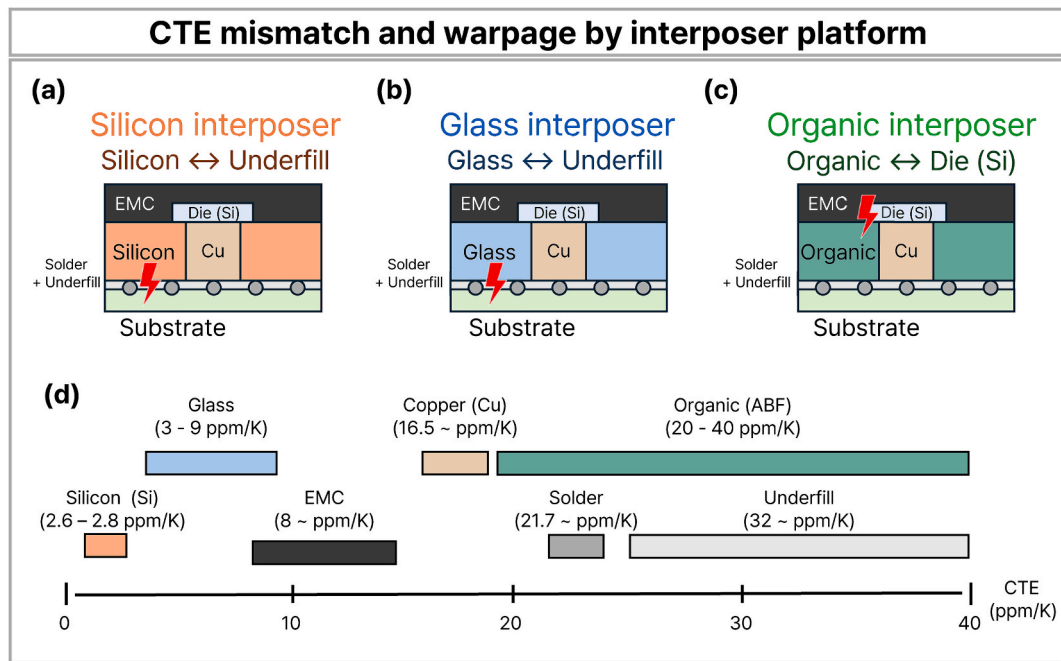


Fig. 10. Dominant CTE mismatch driving warpage in each interposer platform: (a) silicon (silicon–underfill), (b) glass (glass–underfill), (c) organic (organic–die), and (d) representative CTE ranges of the constituent materials [71,89,173–175].

interposer substrate [159].

When similar warpage metrics are applied to glass interposer packaging, the dominant governing variables shift more rapidly from the interposer material to the surrounding stack materials and equivalent structural design [161]. Fig. 9(c) and 9(d) show that warpage distributions can vary markedly with molding material selection, indicating that the commonly cited CTE tunability of glass, in real packages, expands into a CTE-equivalent bending stiffness problem coupled to the CTE, elastic properties, and thickness distribution of molding, underfill, and reinforcement layers [162]. In addition, because glass is brittle, local stress concentrations around the TGV-metal interfaces can be controlled for reliability, even when global flatness and insulation are favorable [163]. Therefore, warpage mitigation in glass-based packaging must be formulated as a coupled optimization across via geometry, pitch, filling architecture, allowable process window, molding/underfill selection, reinforcement design, and stack symmetry, rather than as a flatness-only target [164].

In organic and WLRDL-based packaging, warpage prediction and control are strongly governed by the temperature-dependent properties [165]. Polymers exhibit high CTE and can undergo nonlinear property changes near the glass transition temperature (T_g). Therefore, simulation fidelity can be highly sensitive to small differences in the input property data [166]. Fig. 9(e) and 9(f) demonstrate an inverse calibration approach that extracts the temperature-dependent CTE and reference temperature from warpage measurements and uses them to calibrate simulation inputs, supporting the idea that warpage cannot be reliably described using room-temperature properties and linear elastic assumptions alone [167]. Furthermore, because Cu-polymer multilayer RDL stacks behave as a metal network embedded in a low-stiffness matrix, stress redistribution can become time dependent even under the same temperature excursion, making warpage evolution and interfacial damage tendencies sensitive to process history and operating conditions [168,169].

Consequently, depending on the interposer system, warpage and localized stress concentrations can not only accelerate cracking, delamination, and interconnect fatigue, but also drive progressive increases in contact resistance and variability in parasitic components at micro-bumps, vias, RDL, and metal-polymer interfaces [170]. Therefore,

Table 5

Representative coefficients of thermal expansion of interposer-package constituent materials.

Component	CTE (ppm/K)	Material example	Ref.
Silicon (Si)	2.6 ~ 2.8	Single-crystal Si	[174]
Glass	3 ~ 9	Borosilicate / alkali-free	[89]
Copper (Cu)	16.5	Electroplated Cu	[174]
EMC	8	Silica-filled epoxy	[174]
Solder	21.7	SAC305 (Sn–Ag–Cu)	[175]
Underfill	32	Silica-filled capillary epoxy	[173]
Organic (ABF)	20 ~ 40	Polymer build-up film	[71]
Substrate	17	FR-4 / BT laminate core	[173]

thermo-mechanical behavior should be treated as a coupled limiter that affects not only the structural reliability, but also the electrical performance and operational stability of the package. These warpage and CTE-mismatch behaviors set where stress concentrates, but they do not by themselves indicate how long each platform survives field-representative thermal and humidity excursions, which is ultimately what decides whether a given platform suits a given application. The following subsection therefore moves from these process-induced and static descriptors to standardized accelerated reliability tests, where the same stress concentrations reappear as measurable interconnect fatigue.

In summary, the dominant warpage driver differs markedly across platforms. In silicon TSV interposers, warpage is governed primarily by process-induced residual stress and stacking asymmetry within the multilayer TSV/inter-metal-dielectric composite, amplified as the interposer is thinned and redistributed by micro-bump and underfill constraints, rather than by die-to-interposer CTE mismatch [154,171]. In glass interposers, the controlling factors shift to the CTE, elastic modulus, and thickness of the surrounding molding, underfill, and reinforcement layers [162,172], compounded by local stress concentration at the brittle TGV-metal interfaces, where finite-element analysis indicates that RDL-induced edge cracking is markedly mitigated by adequate edge clearance and by higher-CTE glasses [125]. In organic and WLRDL packages, warpage is dominated by the high, strongly temperature-dependent (near- T_g) CTE and the viscoelastic, time-dependent stress redistribution of the Cu-polymer build-up [127,167].

Table 6

Comparison of accelerated reliability behavior in silicon, glass, and organic/RDL interposers.

Platform	Test & condition	Critical site / failure mode	Quantitative outcome	Type	Ref.
Silicon (TSV / μ bump)	TC, -30 to 125 °C	Micro-bump weakest (bump > TSV-Cu > C4)	Peak bump stress ~ 41.7 % (150 to 87.5 MPa) as thickness 0.1 to 0.3 mm	FEA	[58,60]
Glass (TGV)	TC, -40 to 125 °C	Partial-fill TGV/RDL interface	No cracking after 100 cycles (cycles-to-failure not reported)	Experimental	[82]
Organic / RDL	TC, 0 to 125 °C (JESD22-A104K), 50/50 μ m	Corner RDL delamination + Cu cracking	559 to > 1000 cycles, +10 % life, -61 % warpage (post-anneal)	Experimental	[34]
Organic / RDL fan-out	TC, -40 to 125 °C	Peripheral solder / μ bump creep	Coffin–Manson ≈ 417 cycles, peak von Mises ≈ 147 MPa	FEA	[42,177]

In short, warpage mitigation is principally a constraint- and stack-architecture problem for silicon, a surrounding-stack co-design problem for glass, and a temperature-dependent material (near-Tg) problem for organic substrates. These mechanisms are contrasted schematically in Fig. 10, which also compares the constituent-material CTE values and the resulting mismatch span for each platform.

To make the warpage discussion concrete, Table 5 lists the representative CTE of the package constituent materials shown in Fig. 10. The broad CTE range, from low-CTE silicon and glass up to high-CTE solder, underfill, and organic build-up dielectrics, is what sets the platform-dependent CTE mismatch. However, the contribution of each layer to global warpage also scales with thickness and stiffness, so the thin, compliant solder/underfill layers mainly govern local joint stress rather than package-level warpage.

4.3. Accelerated reliability assessment and quantitative failure behavior

Just as the electrical characteristics of an interposer can be organized systematically to enable rational, application-matched platform selection [176], the reliability requirements that ultimately bind that selection should be evaluated against standardized and mutually comparable criteria. In practice, this evaluation relies on accelerated tests that reproduce field-representative thermal, mechanical, and humidity loading. The most widely reported are temperature cycling (TC; e.g., JESD22-A104), highly accelerated temperature and humidity stress (HAST; JESD22-A110/A118), moisture-sensitivity preconditioning (J-STD-020), and bond or joint shear testing (JESD22-B117). A recurring obstacle to cross-platform comparison is that these methods report different read-outs, namely cycles-to-failure, simulated stress, or mechanical strength. To keep the comparison consistent, the present subsection adopts thermal cycling as a common test axis and CTE-mismatch-driven fatigue of the critical interconnect as a common interpretive lens, and it labels the nature of each data point explicitly. This preserves a like-for-like physical comparison without forcing dissimilar metrics into a single artificial figure of merit.

For organic and RDL interposers, the most complete experimental data set is available (Table 6). Under TC per JESD22-A104K (0– 125 °C) with a daisy-chain resistance-shift criterion of ΔR above 20 % on a 50/50- μ m line/space build, the cycles-to-failure ranged from 559 to more than 1000 depending on the electroplating profile. The dominant failure mode was corner-region interlayer delamination together with copper cracking, and an additional post-deposition anneal improved the fatigue life by about 10 % while reducing warpage by up to 61 % [34]. Panel-level fan-out builds show a similar trend. Thermal-cycling simulations of RDL-first fan-out panel-level packaging (-40 to 125 °C) localized the peak von Mises stress near 147 MPa at the peripheral solder balls and predicted a modified Coffin–Manson fatigue life of about 417 cycles, within roughly 17 % of the experimentally observed value [177]. A complementary hybrid-substrate analysis identified micro-bump creep as the critical accumulation mechanism [42]. Overall, these results identify the peripheral solder joints and corner RDL as the weakest links of organic and RDL platforms, and they show that reliability is strongly modulated by process and anneal history.

For silicon interposers, the publicly reported quantitative reliability

data remain mostly simulation-based (Table 6). Finite-element analysis (FEA) under TC (-30 to 125 °C) identifies the micro-bumps beneath the interposer as the weakest link, carrying the highest equivalent stress relative to the TSV copper and the C4 joints [60]. Parametric studies further report that increasing the interposer thickness from 0.1 to 0.3 mm lowers the peak bump stress by about 41.7 %, from roughly 150 to 87.5 MPa [58]. These analyses are internally consistent and physically informative. At the same time, measured cycles-to-failure on silicon-interposer test vehicles are comparatively scarce in the open literature, and this gap is reported here rather than filled with values obtained under dissimilar test conditions.

For glass interposers, the most directly comparable thermal-cycling result is a partially filled TGV and RDL structure formed by double-sided conformal copper electroplating (Table 6). It showed no cracking or protrusion at critical locations after 100 cycles between -40 and 125 °C, although a standardized cycles-to-failure under a defined resistance-shift criterion was not reported [82]. As a complementary long-term indicator, TGV-based vacuum packages have sustained an internal pressure near 1 Pa for more than two years, indicating stable through-glass interconnection and sealing over field-relevant timescales [82]. A separate measure that lies outside the thermal-cycling axis is the solder-joint shear strength of glass and TGV assemblies (JESD22-B117), which rose from about 72 to a peak of 96 MPa and then fell to about 47 MPa as the shear rate increased. This change was accompanied by a ductile-to-brittle transition above 10 mm/s, with failure shifting to copper-pad lift-off, RDL peel-off, and glass fracture [26]. It is reported here as a complementary measure of joint-level mechanical robustness rather than as a thermal-fatigue equivalent.

Taken together, Table 6 shows that the limiting element is platform-specific rather than universal. It is micro-bumps for silicon, the corner RDL and peripheral solder joints for organic and RDL builds, and for glass a combination of demonstrated cycling capability and long-term hermeticity that is offset by a scarcity of standardized test-vehicle fatigue data. To avoid possible overinterpretation, this comparison is presented as representative of reported platform behavior rather than as a single calibrated benchmark, because test-vehicle geometries, loading profiles, and resistance-shift criteria differ across the cited studies. A further cross-cutting observation is that quantitative HAST, unbiased-HAST, and moisture-sensitivity data on interposer test vehicles remain comparatively scarce for all three platforms in the open literature, so standardized cross-platform humidity-reliability reporting is identified here as an open requirement. These platform-dependent weakest links, together with the warpage signatures of Section 4.2, frame the electrical-integrity discussion that follows and the long-term multi-material interface-stability challenge discussed in Section 7.1.

5. Electrical integrity analysis of interposers

Interposer stacks operate under repeated thermal excursions, and the thermo-mechanical behaviors discussed in Section 4 continuously influence the electrical environment of the package. Warpage and stress-driven interfacial degradation can modify the interconnect geometry and contact conditions, leading to drift and nonuniformity in parasitic elements that govern channel loss, crosstalk susceptibility, and

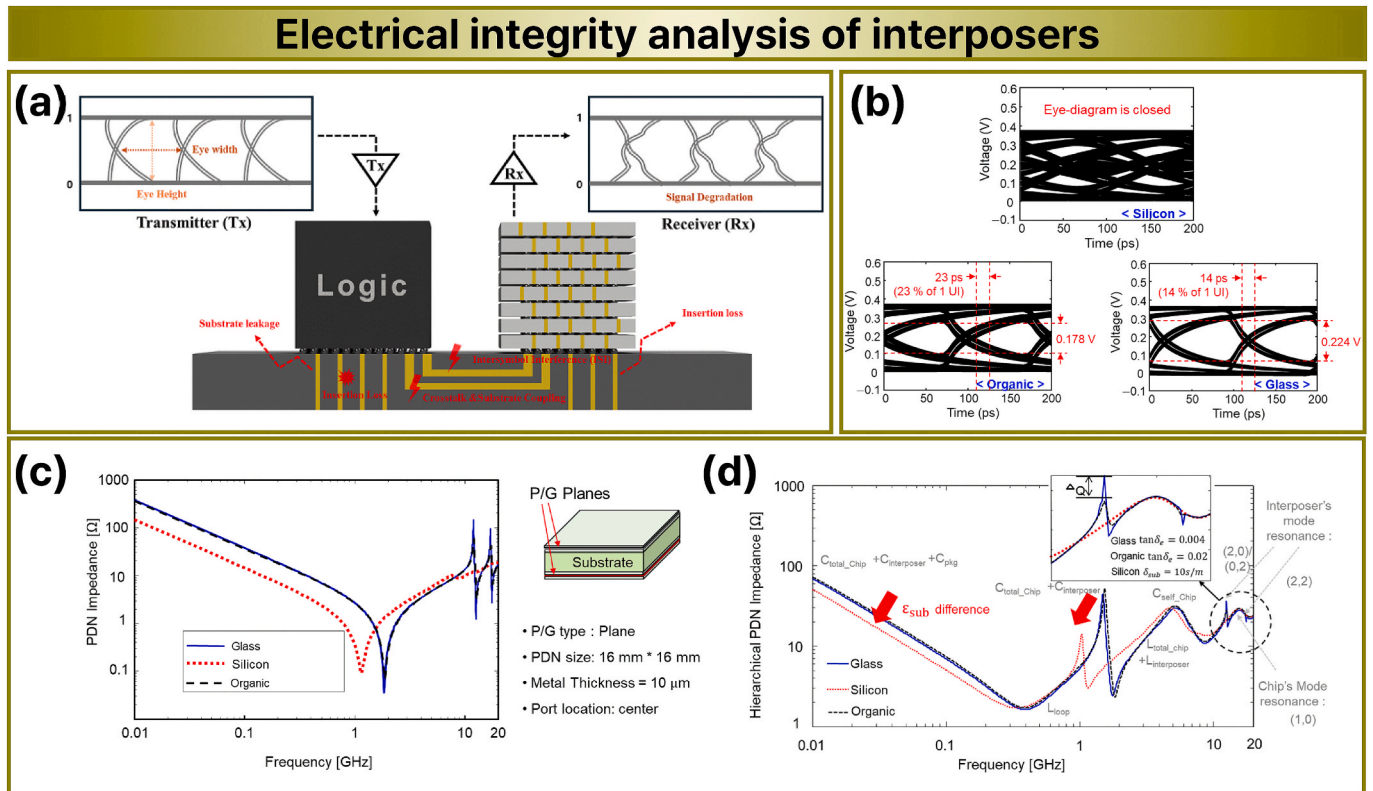


Fig. 11. SI and PI of interposers: (a) Tx-Rx channel and key signal loss, (b) eye diagrams by material (representative of typical platform configurations rather than a strictly calibrated benchmark, as channel length, routing-layer count, and via count are not necessarily identical across the three materials). Adapted from [179] under the terms of the Creative Commons CC BY license, (c) PDN impedance. Adapted from [179] under the terms of the Creative Commons CC BY license, and (d) resonance behavior. Adapted from [179] under the terms of the Creative Commons CC BY license.

resonance behavior. Consequently, electrical integrity analysis should be framed as a coupled outcome of material choice, process-induced residual states, and stack-level constraints rather than as a stand-alone electromagnetic problem. Interposers support a wide bandwidth, low latency, and high-power efficiency by enabling dense, close-proximity interconnects through vertical vias [178]. Although these advantages have historically driven industrial interest in silicon interposers and TSV, inherent limitations, such as wafer-size constraints and the conductive nature of silicon substrates, have motivated the exploration of alternative materials [179]. Consequently, maximizing the benefits of practical packaging requires a precise understanding of the electrical behaviors of various interposer types to ensure a rational selection that matches specific application requirements. For instance, to apply interposers in 2.5D chiplet integration, the design must comply with the Universal Chiplet Interconnect Express (UCIe) specification, which requires organizing electrical characteristics into two systematic categories: channel SI and PI, including the power delivery network (PDN) [176].

Beyond this thermo-mechanical coupling, a second and increasingly dominant cross-domain effect is thermo-electrical coupling, which we highlight as a forward-looking, systemic challenge for high-power-density interposers. The thermal and electrical domains are bidirectionally linked: Joule self-heating in vias, the RDL, and the PDN raises the local temperature, while the resistivity of copper and the loss tangent of the dielectrics are themselves temperature-dependent, so heating increases IR drop, insertion loss, and current crowding, which in turn generate further heating, a positive electrothermal feedback loop. In 2.5D/3D stacks that dissipate hundreds of watts per package and form localized hotspots, this feedback directly limits achievable performance and accelerates temperature- and current-driven failure mechanisms such as electromigration at vias and micro-bumps [124,140]. The

coupling is further aggravated on non-silicon platforms, where the lower thermal conductivity of glass and organic dielectrics forces heat removal and signal/power routing to compete within the same structure. Addressing it requires treating thermo-electrical behavior as an explicit co-design axis rather than as sequential thermal and electrical sign-offs. Representative mitigation routes include electrothermal co-optimization of the power-delivery network [180], thermal through-vias and embedded micro-channel/micro-fluidic cooling [140,181,182], thermally aware floor planning and back-side power delivery, and the use of low-loss dielectrics with higher effective thermal conductivity. We therefore identify thermo-electrical co-design as a key enabler for next-generation, high-power-density interposers.

5.1. Signal integrity of interposers

In 2.5D/3D integration, SI becomes a primary design requirement because rising data rates and I/O densities amplify the channel loss and inter-channel coupling, which directly manifest as eye-diagram degradation at the receiver [183]. The transmission process can be framed using transmitter (Tx) and receiver (Rx) roles, as shown in Fig. 11(a). Tx launches a high-speed waveform into the channel, and Rx reconstructs digital data from the received waveform. The eye diagram quantifies the reconstruction margin by overlaying the received waveforms over a unit interval. The eye height represents the voltage margin, and the eye width represents the timing margin. As channel impairment increases, eye closure occurs via three coupled mechanisms. First, the insertion loss driven by routing/via resistance and dielectric loss preferentially attenuates high-frequency components, reducing transition sharpness and reducing eye height. Second, a high routing density increases the electromagnetic coupling between adjacent channels, injecting crosstalk noise that simultaneously erodes the voltage and timing margins. Third,

bandwidth limitation and reflection generate inter-symbol interference (ISI), allowing the residual energy from previous bits to overlap with subsequent bits and narrow the eye width [184]. Because the associated electric and magnetic fields largely reside within the interposer substrate and its immediate dielectric environment, SI becomes highly sensitive to both material loss and structural configuration. Consistent with this coupling, Fig. 11(b) shows that, at the same 10 Gb/s data rate, different interposer materials yield distinct eye openings [179], which motivates material-specific SI optimization strategies. These eye diagrams are reproduced from a single comparative study and are intended to illustrate differences among typical platform configurations rather than a strictly calibrated benchmark. The channel length, the number of routing layers, and the number of vias are not necessarily identical across the three materials, so the comparison should be interpreted as representative of typical platform configurations rather than as a controlled one-to-one measurement.

Silicon interposers offer a high I/O capacity [185]. However, two structural characteristics drive SI penalties at the frequency and routing scales. Reticule limitations constrain lateral scaling [186], and the lossy silicon substrate, together with the surrounding dielectric loss, increases high-frequency insertion loss and waveform distortion [187]. These loss mechanisms translate into reduced eye stability relative to other interposer platforms, as shown in Fig. 11(b) [179]. At HBM-class data rates, similar loss/coupling mechanisms interact more strongly with crosstalk and ISI, thereby tightening the eye margin. To reduce substrate-coupling-related penalties, silicon dioxide wells (SDWs) have been introduced to suppress leakage paths and reduce the parasitic capacitance around the TSVs, producing eye-diagram improvements and a 48.1 % reduction in power consumption for the HBM Gen3 and Gen4 conditions [188]. Passive equalizers inserted between the TSV and RDL compensate for the preferential loss of high-frequency content and mitigate reflections, thereby recovering the eye margins [189]. As SI optimization becomes increasingly multidimensional, surrogate model-based approaches using DNN and KBNN trained on EM/Q2D data have been adopted to predict channel characteristics and quantify the impact of routing geometry without repeated full-wave simulations, thereby accelerating design iterations under tight eye-margin constraints [184].

Organic interposers based on dielectric substrates, such as ABF, support large-area panel processing and reduce costs, and their low dielectric constants and loss tangents can yield lower insertion losses than silicon-based channels [183]. However, the limited dimensional stability and CTE mismatch complicate fine routing and high-density I/O realization, making SI not only a material issue but also a manufacturability-constrained routing problem [190]. RDL interposers address this scaling pressure by shifting the primary design leverage to the routing architecture and return-path engineering. For example, the chip-on-wafer-on-substrate s-RDL platform distributes channels across multiple RDL layers and employs signal-ground-signal routing to suppress coupling while maintaining a high routing density, directly improving the SI without requiring a low-loss bulk substrate [191]. Beyond line shielding, mesh-type ground planes allow impedance and coupling to be controlled through pattern design. Diagonal routing has been shown to reduce crosstalk compared with horizontal patterns at the same pitch, indicating that the routing orientation becomes an SI knob [192,193]. As this design space becomes combinatorial, reinforcement learning has been explored to identify trace dimensions that preserve eye margins while increasing I/O density, effectively treating SI closure avoidance as an optimization target under routing density constraints [194].

Glass interposers are attractive for SI applications because their high resistivity and low dielectric loss reduce attenuation and dispersion even at high frequencies [195]. This low-loss condition translates into visibly wider eye openings. Reported results show a 64.7 % SI improvement compared with alternative technologies and the widest eye margins in the logic-to-memory paths [196]. However, glass introduces a different set of constraints, in which process- and reliability-driven defects can be

converted into SI degradation. Brittleness increases the risk of cracking, motivating the development of polymer-coated thin-film glass interposers that preserve low insertion loss while improving crack resistance [197]. In addition, TGV formation can introduce surface roughness that exacerbates high-frequency distortion via the skin effect, increasing the effective conductor loss and degrading the waveform despite the intrinsically low-loss substrate. Vector network analyzer-based measurements with RLGC extraction indicate that maintaining smooth, cylindrical via walls and minimizing alignment errors are essential for preserving the inherent low-loss advantages of glass in practical channels [198,199].

Overall, in an interposer, SI must be improved to address problems such as channel loss, crosstalk, and ISI [200]. Silicon platforms prioritize reducing substrate/TSV-related loss and coupling, organic/RDL platforms rely on return-path and routing-architecture optimization under manufacturability constraints, and glass platforms preserve low-loss behavior while controlling brittleness and process-induced TGV imperfections.

5.2. Power integrity and power delivery networks of interposers

PI evaluates the stability of the supply voltage delivered to the operating chip, and the impedance profile of the PDN, which is $Z(f)$, serves as the primary metric [201]. The PDN forms a hierarchical path from the on-chip interconnects through packaging and interposer structures to board-level decoupling capacitors [202]. When anti-resonance occurs along this path, simultaneous switching noise (SSN) can be amplified, destabilizing the chip operation, even when the average DC delivery appears adequate [203]. In this framework, Fig. 11(c) and (d) show that the PDN impedance behavior is strongly material and structure dependent. Glass interposers exhibit the sharpest impedance peaks, whereas other platforms show impedance profiles shaped by their specific parasitic RLC networks and loss mechanisms [179]. This implies that PI is governed not only by “how low the loss is,” but by how loss and parasitics collectively set the quality-factor (Q-factor) and modal resonance strength across frequency.

Silicon interposers behave as lossy parallel-plate structures because bulk silicon introduces dielectric and conduction losses. This loss mechanism lowers the Q-factor of the resonant modes, which can suppress extreme anti-resonance amplification and maintain a relatively moderate impedance behavior, even at large lateral dimensions [204]. Circuit-based hierarchical modeling that discretizes the PCB, package, interposer, and on-chip regions into RLC elements further supports the idea that substrate loss prevents sharp peaking of the resonance [205]. Stepwise segmentation of large-area PDNs into on-chip, TSV, and interposer sections shows that silicon substrate loss tends to smoothen the impedance curve and avoid sharp resonance spikes [206]. In addition to passive damping, active interposer PDNs have demonstrated dynamic SSN reduction by shifting the anti-resonance frequencies via switch-controlled decoupling capacitor connections, effectively using reconfigurable impedance as a PI control method [207]. Similarly, in 3D SiP structures employing TSV interposers, the inherent loss characteristics of silicon have been reported to suppress the fatal PDN resonance in large-area packages [208]. The trade-off is that the same loss that damps resonances also dissipates energy. Thus, in low-power systems, where maximizing the power efficiency is critical, the silicon substrate loss and TSV resistance/inductance can become non-negligible penalties.

Organic interposers using materials such as liquid crystal polymers can achieve low PDN impedance and favorable power efficiency owing to their low permittivity and thick copper routing, enabling wide PDN planes during panel processes [209,210]. However, as the frequency increases, the transmission line behavior and losses in fine RDL routing increasingly shape the high-frequency PDN impedance, and the placement of the limited decoupling capacitors in high-density organic packaging can make anti-resonance frequencies highly sensitive to small

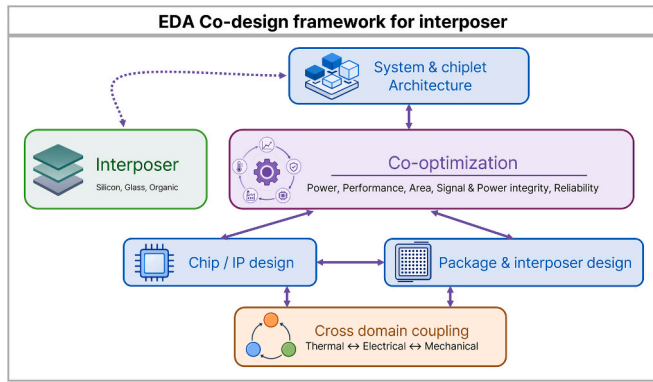


Fig. 12. EDA-driven co-design framework for interposer-based 2.5D/3D integration [180,197,219,220].

structural variations [211]. To compensate for limited effective plane capacitance, interdigital capacitor (IDC) patterning and high-k material insertion have been proposed to increase distributed capacitance by

turning the interposer into an effective decoupling structure, directly shifting the PDN from a “low-impedance plane” concept toward an “embedded capacitance” concept [212,213].

Glass is generally ideal from the SI viewpoint because its low dielectric loss preserves the signal waveforms. However, similar low-loss nature increases the Q-factor of the PDN resonances, making the resonance peaks sharper and more numerous from the PI viewpoint. Comparative studies with identical geometries have shown that glass PDNs can exhibit higher Q-factor behavior with multiple sharp impedance peaks across modes, and that power/ground noise and eye-diagram degradation can be simultaneously observed at these resonance frequencies [214]. This behavior is attributed to the cavity-like standing-wave resonances supported by the low-loss parallel-plane structure and its coupling with the TGV/patch features across the interposer [215]. Consequently, glass PDN design requires deliberate resonance-suppression structures. The reported strategies include mushroom-type electromagnetic bandgap insertion between the power/ground planes to block noise transmission over the targeted bands [216] and the surrounding signal TGV with multiple ground TGV to reduce resonance-mode noise coupling [25]. Recent methodologies emphasize defining

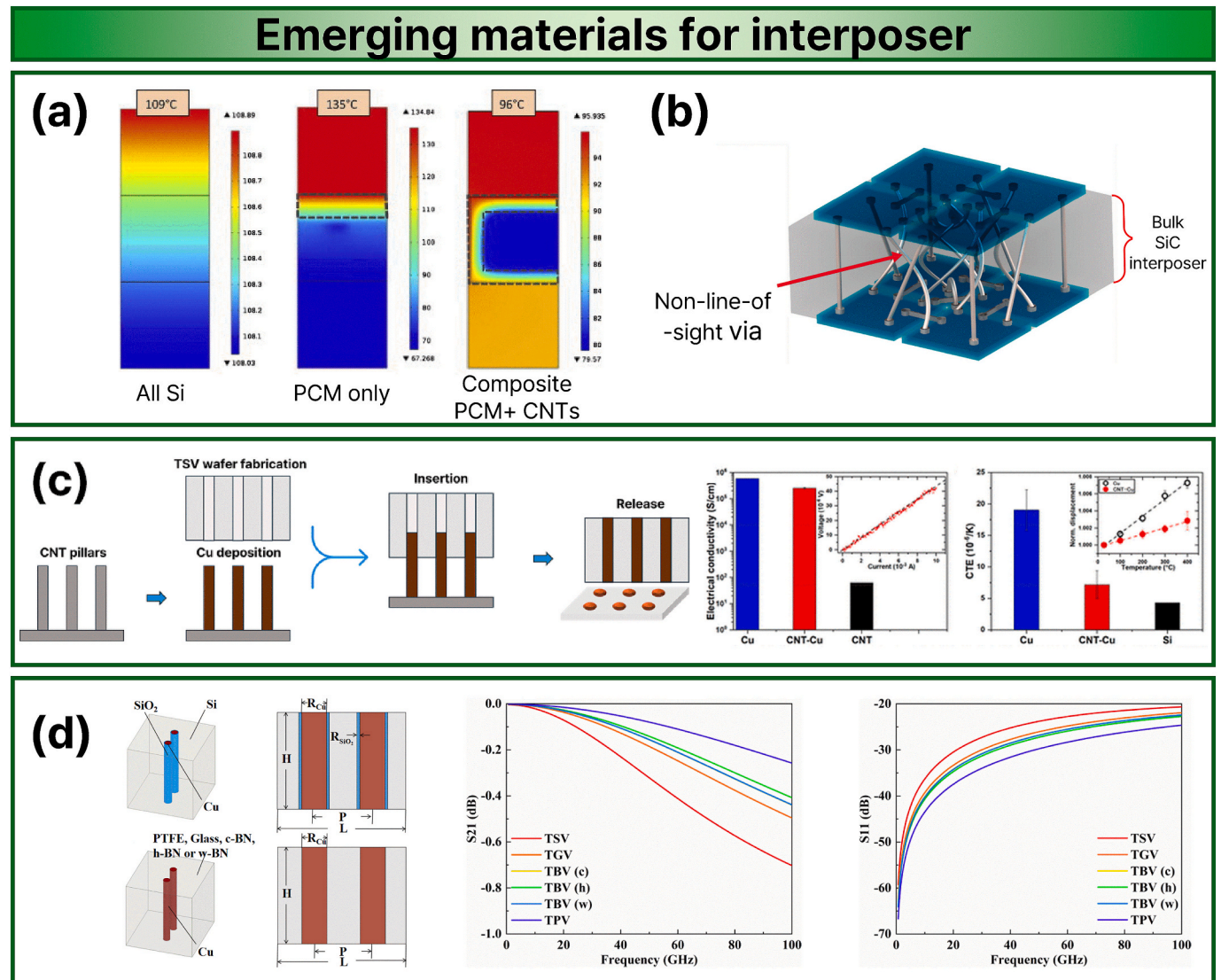


Fig. 13. Emerging materials and architectures for next-generation interposers: (a) PCM/CNT-assisted thermal buffering for transient hotspot mitigation. Adapted from [226], (b) 3D via/routing reconfiguration using non-line-of-sight TWV concepts. Adapted from [227] under the terms of the Creative Commons CC BY license, (c) CNT-Cu composite conductors for reduced CTE mismatch while retaining high conductivity. Adapted from [228], and (d) SI-oriented redesign of via insulation/materials to tailor high-frequency parasitics. Adapted from [229].

frequency-specific target impedances aligned with realistic switching spectra and performing hierarchical PDN analysis, thereby avoiding the inefficient strategy of forcing a uniformly low impedance over all bands [217]. Importantly, even the inherent SI advantage of glass can be compromised if the PDN resonance is not sufficiently controlled, as eye damage can occur through supply-noise-induced timing/voltage margin loss [218].

Overall, PDN behavior differs fundamentally by interposer type because each platform embeds a distinct combination of parasitic networks and loss mechanisms. Therefore, no single material has a universal PI advantage across all frequency bands. Instead, interposer selection and PDN design must be aligned with system priorities such as power efficiency, resonance suppression, and signal bandwidth, and these priorities often require different trade-offs across platforms.

5.3. Design-automation and co-design considerations

Beyond material and process considerations, interposer platform selection is increasingly a system-level co-design problem in which power, performance, and area (PPA) are traded against signal and power integrity (SI/PI), thermal behavior, and reliability, as illustrated in Fig. 12, which also summarizes the platform design trade-offs and the underlying thermal–electrical–mechanical coupling. As summarized in Fig. 12, this co-design view links the interposer-platform choice with three coupled design stages, namely system/chiplet architecture, chip/IP design, and package/interposer design, which are optimized together against the shared objectives of PPA, signal/power integrity, thermal behavior, and reliability rather than in isolation. Recent design-automation studies have quantified these trade-offs across platforms. Glass interposers have been shown to provide measurable PPA and signal/power-integrity benefits for logic–memory chiplet integration relative to a silicon-interposer baseline, reporting, for a logic–memory chiplet case, roughly $2.6 \times$ smaller area, $\sim 21 \times$ shorter wirelength, $\sim 18\%$ lower full-chip power, and substantial signal- and power-integrity gains [197], while broader electronic design automation (EDA) studies of heterogeneous 3D-integration options have clarified the power–performance–cost trade-offs and the design-automation solutions required for each scheme [180]. At the flow level, dedicated clock- and power delivery network co-design for interposer-based 2.5D systems demonstrates that interposer choice, redistribution routing, bump pitch, and network topology must be optimized jointly rather than in isolation [219]. Recent work further applies machine learning to optimize bump-pitch and interconnect design quality [220]. Incorporating such EDA-driven co-design perspectives is essential for translating the material- and fabrication-level differences surveyed above into realized system-level performance.

6. Emerging materials for interposer

The performance limits of interposer-based packaging are not determined solely by intrinsic substrate properties but emerge from the coupled effects of the metal volume fraction in via/routing architectures, interfacial quality, process thermal history, and constraint conditions imposed by the surrounding stack materials [221–223]. In advanced 2.5D/3D packages integrating high-power logic and HBM, these coupled factors first determine the heat dissipation pathways and thermo-mechanical responses, and the resulting deformation and interfacial drift can subsequently disturb the parasitic elements that govern the stability of electrical integrity [224,225]. In this context, recent studies have largely retained the conventional classification of interposers into silicon, glass, and organic platforms, while focusing on strategies that bypass system-level bottlenecks through material substitution or structural redesign, as illustrated in Fig. 13.

Fig. 13(a) illustrates an approach that introduces a phase-change material (PCM) within the interposer to mitigate the transient temperature peaks by altering the storage and redistribution of heat under

pulsed loading. In pure silicon, the temperature rise is moderated primarily through heat spreading into the bulk silicon, whereas filling the cavity solely with a PCM can hinder heat transfer into the underlying silicon because the PCM layer provides a low-conductivity path, causing heat to accumulate locally near the top region and accelerating the local temperature rise. When carbon nanotubes (CNTs) are incorporated into the PCM, additional conduction pathways increase the effective heat spreading within the cavity. Thus, PCM melting is no longer confined to an upper localized region but occurs over a larger volume, while the heat transfer into the underlying silicon is simultaneously enhanced. This suggests that the PCM/CNT hybridization extends the role of the interposer beyond mere structural support to an architecture-level thermal buffer that suppresses the temperature peaks under thermal pulse conditions [226]. Fig. 13(b) shows a strategy that targets electrical bottlenecks by reconfiguring the via/routing topology in three dimensions rather than attempting an incremental refinement of planar routing. When multiple chiplets are directly interconnected using conventional low-aspect-ratio, line-of-sight vias combined with a simple double-sided RDL, constraints on insulation spacing and routing width force lateral routing to spread and detour, enlarging the interposer footprint and increasing the inter-chiplet interconnect length, thereby exacerbating latency and channel loss. In contrast, the through-wafer via (TWV) concept enables high-aspect-ratio, non-line-of-sight, and interwoven via configurations that allow paths, which would otherwise detour in a 2D plane, to be reconfigured into more direct three-dimensional routes, enabling equivalent connectivity within a smaller footprint. Although longer, higher-aspect-ratio vias inevitably increase the DC resistance, shortening the overall interconnect path length can still provide a net system-level benefit by reducing the delay and loss associated with extended routing [227]. Fig. 13(c) shows a representative example in which the repeated CTE mismatch in TSV/TGV filling is addressed by modifying the thermo-mechanical properties of the filling conductor, rather than only pursuing defect-free deposition. CNT-Cu composite pillars have been observed to maintain Cu-like electrical conductivity while exhibiting a markedly reduced CTE that closely matches that of Si, thereby mitigating the CTE mismatch. This implies that the reduced expansion and contraction during thermal cycling can alleviate the thermally induced deformation and interfacial stress concentrations around the vias. Although many prior studies have focused primarily on achieving void-free Cu filling, this approach advances the design space by treating the filling metal as a tunable thermo-mechanical element with direct implications for stress evolution and reliability [228]. Fig. 13(d) illustrates a high-frequency SI-driven approach in which the insulation structures and via types are redesigned to reshape the parasitic components under identical geometric constraints. The key finding is that the material and insulation choices modify the parasitic capacitance, conductance, and field confinement, and these changes manifest as distinct loss characteristics. Adopting materials with superior insulating properties, such as cubic boron nitride, can yield an improved SI compared with conventional TSV and TGV by shifting the parasitic balance in a direction favorable for low-loss, low-coupling behavior [229].

In summary, the four cases shown in Fig. 13 illustrate different research directions. However, they share a common logic: each identifies a dominant platform bottleneck, introduces a material or architectural change to alter the governing transport or parasitic mechanism, and realizes the performance headroom as an improved thermal response, SI margin, or reliability tolerance. However, because these approaches must simultaneously satisfy practical constraints such as process compatibility, large-area uniformity, long-term reliability, and cost/yield considerations, they can introduce new trade-offs in manufacturability and package-level integration alongside performance improvements. Therefore, further advances in scalable fabrication and integration strategies are required to translate these emerging materials and architectural concepts into production-relevant interposer solutions.

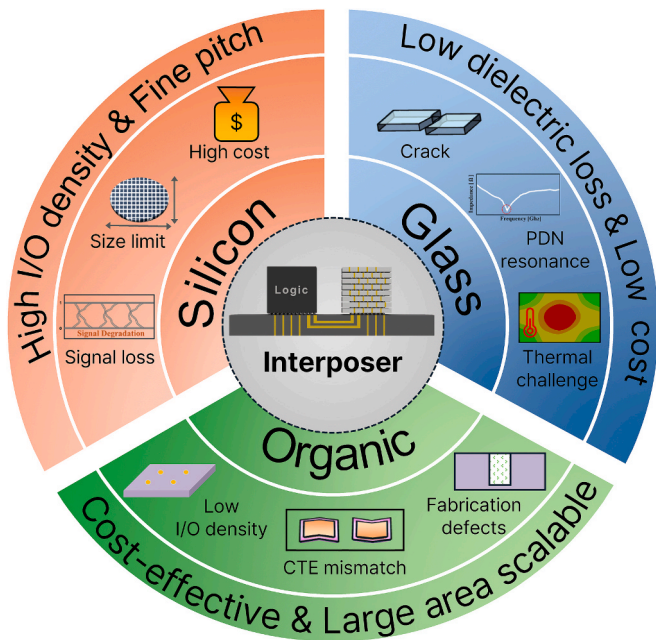


Fig. 14. Key challenges for silicon, glass, and organic interposers in 2.5D/3D advanced packaging.

The four directions in Fig. 13 differ not only in their mechanisms but also in how far they have progressed toward manufacturing, and distinguishing these maturity levels helps separate near-term expectations from longer-term prospects. On a simple maturity scale ranging from concept and modeling, through experimental proof-of-concept at the coupon or single-structure scale, to qualified prototypes, low-volume pilot production, and finally volume production, the present cases remain at the early end. The PCM/CNT thermal buffer [226] and the cubic-boron-nitride-based via redesign [229] are supported mainly by thermal and electromagnetic modeling, placing them at the concept/modeling stage. The Through-Wafer-Via routing scheme [227] is presented as an architectural concept whose benefits are evaluated at the system level rather than demonstrated on a fabricated test vehicle, placing it at a comparable early stage. The CNT-Cu composite pillar [228] is the most advanced of the four because its reduced CTE and near-copper conductivity have been experimentally observed, placing it at the lab-scale proof-of-concept stage. None of these approaches, however, has yet been reported at the level of a qualified prototype, pilot-line demonstration, or volume manufacturing, and each still faces the scaling barriers noted above, namely process compatibility, large-area uniformity, long-term reliability, and cost and yield. This stratification is necessarily approximate, as it reflects the nature of the reported evidence rather than formal qualification data, but it clarifies why these materials are treated in Section 8 as longer-term directions, whereas near-term practice continues to rely on established silicon, glass, and

organic/RDL platforms, together with bridge-embedded hybrids.

7. Key challenges for interposers

Recently, the rapid development of HBM and chiplet-based heterogeneous integration has intensified research into interposer technologies that enable large-area, high-density routing. As key package-level structures, interposers provide high-density signals and power delivery between dies and package substrates, thereby leveraging material-specific advantages while mitigating inherent limitations. Fig. 14 shows the key challenges that must be addressed to realize these benefits and overcome the major limitations of interposer platforms.

• Silicon interposer

- Silicon interposers fabricated from silicon wafers are the most widely used 2.5D/3D packaging platforms because of their high micro-fabrication precision, strong compatibility with complementary metal oxide semiconductor processes, and stable mechanical and thermal behaviors. They support HBM interconnects through TSV and multilayer RDL. The planar silicon surface and fine-pitch wiring enable high micro-bump counts, small pitches, and high routing densities. However, manufacturing challenges remain, such as void formation during TSV filling, increased via resistance, process constraints for fine-pitch RDL, and stress-induced reliability degradation. Furthermore, scaling to large-area interposers is constrained by the reticle size, and a lossy silicon substrate can introduce high-frequency insertion losses and distortions. Parasitic TSVs further degrade the SI. The intrinsic substrate losses also lower the Q factor of the PDN modes, which can mitigate the resonance severity at the package scale.

• Glass interposer

- Glass interposers offer high electrical insulation and favorable dielectric properties, such as a low dielectric constant and low loss, making them highly attractive for high-frequency operations. Their CTE can be tailored through compositional engineering, which may help mitigate thermo-mechanical mismatch and warpage in heterogeneous stacks. However, the inherent brittleness of glass makes it susceptible to microcrack formation during the TGV processing. These microcracks can propagate during the subsequent processing steps and thermal loading, leading to reliability concerns. The low dielectric loss of glass can increase the Q factor of package-level PDN modes, which may exacerbate the resonant impedance peaks in the PDN.

• Organic interposer

- Organic interposers extend the conventional package-substrate technology by stacking built-up dielectric layers on an organic core to form multilayer wiring. This makes them attractive owing to their cost advantages and suitability for large-area panel-level manufacturing. However, polymer-based materials pose significant challenges in terms of warpage suppression, primarily owing to the CTE mismatch and ultrafine routing. In addition, at millimeter-wave frequencies, process variations and surface roughness can increase

Table 7

Summary of representative advantages, suitable applications, practical limitations, and cost and scalability of silicon, glass, organic/RDL, and hybrid bridge-embedded interposers.

Platform	Distinctive achievement	Best-fit application	Limiting factor	Cost / scalability
Silicon (TSV)	Finest pitch, highest I/O density, mature CMOS, HBM (TSV + RDL)	Logic-HBM, max routing density	Reticle-limited area, lossy substrate, μbump weakest link [60]	High cost, reticle-limited scaling
Glass (TGV)	Low RF loss (<1.8 dB), tailorable CTE, optically transparent [46]	mmWave / RF front-ends, low-loss channels	Brittle, TGV microcracks, TGV-metal stress, high-Q PDN anti-resonance [214]	Moderate, panels feasible, TGV + RDL add cost
Organic / RDL	Panel-scale low-cost build-up (SAP), RDL fine routing	Cost/area-driven volume, moderate performance	High CTE/warpage, fine-routing limit, mmWave loss	Lowest cost, highest manufacturability
Hybrid bridge (EMIB / CoWoS-L)	Silicon-class local routing on large organic area [51,52]	Large-area chiplet integration with local high-density links	Bridge-organic CTE mismatch, cavity/placement yield	Relaxes silicon cost/reticle, added assembly complexity

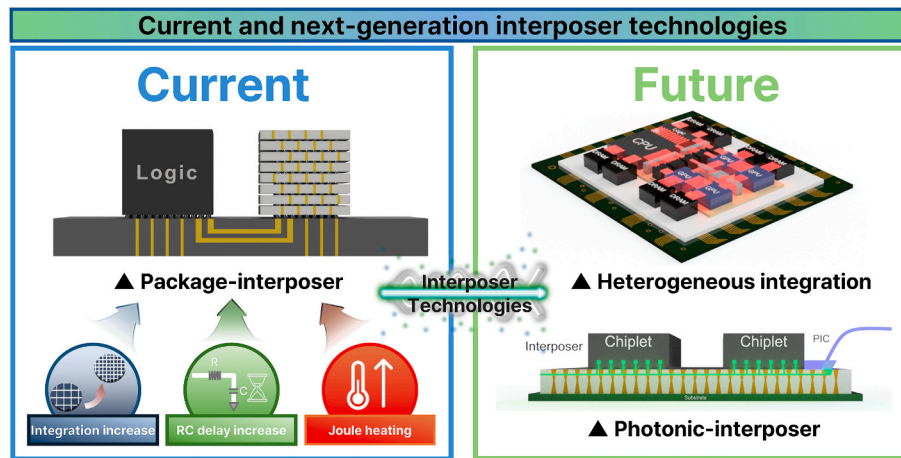


Fig. 15. Current and next-generation interposer technologies: current electrical interposer-based integration and scaling limits and next-generation hybrid interposers for chiplet and co-packaged optics.

losses, potentially degrading the high-frequency performance. Overall, their practical design is constrained by a three-way co-design trade-off between routing density, thermo-mechanical warpage, and cross-plane thermal resistance.

Each interposer platform has distinct strengths and limitations. Further progress is expected to be driven by process optimization tailored to material properties and co-design approaches that jointly consider the thermal, mechanical, and electrical requirements to achieve high-performance and scalable manufacturability.

Although the preceding sections discuss the properties, fabrication processes, and reliability issues of each interposer platform separately, their practical selection should be considered in relation to the target application and the dominant design constraint. Table 7 summarizes the representative advantages, suitable applications, practical limitations, and cost/scalability of silicon, glass, organic/RDL, and hybrid bridge-embedded interposers. Silicon interposers provide the finest routing pitch and the highest I/O density, making them suitable for high-bandwidth logic-to-memory integration such as HBM-based high-performance computing (HPC) and AI packages. However, their application is limited by reticle size, high fabrication cost, and substrate-related electrical loss. Glass interposers are advantageous for low-loss signal transmission and are therefore promising for millimeter-wave and RF applications, although brittleness and TGV-related interfacial stress remain major reliability concerns. Organic/RDL interposers offer low cost, large-area processability, and high manufacturability, but their use in ultra-fine-pitch applications is limited by warpage, dimensional stability, and routing resolution. Hybrid bridge-embedded interposers provide a compromise between silicon and organic/RDL platforms by placing silicon-class routing only in local regions where high-density interconnects are required. However, this architecture introduces additional challenges related to bridge-to-organic interfacial reliability, bridge placement accuracy, and assembly yield. Therefore, these interposer platforms should be regarded as complementary options, and the final platform selection should be determined by the dominant requirement of the target system, such as routing density, signal loss, package size, cost, or thermo-mechanical reliability.

7.1. Cross-cutting challenge: long-term stability of multi-material interfaces

Beyond the platform-specific challenges summarized above, long-term stability of multi-material interfaces remains a common reliability issue across all interposer technologies. Regardless of the base substrate, interposers rely on stable adhesion and electrical continuity at

interfaces between metals, dielectrics, and substrates. In silicon interposers, stress concentration can occur around TSV, micro-bump, and underfill-related interfaces [60,159]. In glass interposers, the TGV-metal interface becomes critical because brittle glass is sensitive to crack initiation and interfacial stress [111,163]. In organic/RDL platforms, the Cu-polymer interface and corner RDL regions are susceptible to delamination, Cu cracking, and resistance increase [34,121]. In bridge-embedded hybrid architectures, the bridge-to-organic interface introduces an additional CTE-mismatch region [54]. Under long-term thermal cycling, humidity, and electrical loading, these interfaces can degrade through interdiffusion, oxidation, moisture-assisted adhesion loss, stress migration, and electromigration, eventually leading to delamination, cracking, or contact-resistance drift. Therefore, interface stability should be treated as a shared research gap rather than as a platform-specific issue alone. Future work should focus on standardized interface characterization, accelerated interface-degradation tests, and interface-aware material/process co-design to improve package-level lifetime.

8. Conclusion and future outlook

The semiconductor industry's long-established reliance on transistor geometry scaling to drive performance has approached its fundamental limits. As physical limits and increasing costs render traditional scaling less viable, attention has shifted toward "Beyond Moore" strategies that emphasize system-wide innovation [230]. Heterogeneous integration via chiplet-based designs is crucial to this transition. Rather than relying on device-level shrinkage, this approach leverages architectural partitioning and integration to improve performance and position interposers as key enabling platforms for modern 2.5D and 3D systems [231]. A range of interposers, including silicon, glass, and organic, have emerged to address diverse packaging requirements. However, as the integration density increases, these platforms experience increasingly similar constraints. As shown in Fig. 15, the electrical interconnect scaling is the primary bottleneck. Increased wiring resistance and RC delay and the associated Joule heating can erode gains in bandwidth and power efficiency [232,233]. These trends suggest that the incremental optimization of conventional electrical routing methods will yield diminishing returns. As the thermal and electrical constraints intensify, engineers are forced to reconsider the significance of the interposers. This surpasses the scope of the passive wiring of the substrates. Co-packaged optics exemplify this shift by integrating optical interfaces within the package to reduce the distance that signals must traverse copper interconnects [234]. In this context, the interposers serve as heterogeneous integration platforms for logic chiplets and photonic components. Glass is a strong

candidate for these applications because it is optically transparent and possesses favorable electrical properties such as high insulation and low dielectric loss, although challenges related to brittleness and thermal management at scale must still be addressed.

In conclusion, industries are unlikely to converge on a single interposer. Success in the Beyond-Moore era will depend on a rigorous multiphysics co-design process. This means jointly considering the SI, thermal management, and emerging optical I/O pathways. Such an integrated design is critical for extending system-level scaling beyond its current limits and enabling heterogeneous electronic-photonics architectures.

CRedit authorship contribution statement

Yonghyun Kim: Writing – original draft, Methodology, Investigation, Formal analysis, Conceptualization, Data curation, Visualization, Writing – review & editing. **Hoyoon Lee:** Writing – original draft, Visualization, Methodology, Investigation, Formal analysis, Conceptualization, Data curation, Writing – review & editing. **Jeongwoo Park:** Investigation, Data curation. **Sangmin Cho:** Data curation, Investigation. **Hongyun So:** Writing – review & editing, Supervision, Resources, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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