

Analog Synaptic Devices Based on IGZO Thin-Film Transistors with a Metal–Ferroelectric–Metal–Insulator–Semiconductor Structure for High-Performance Neuromorphic Systems

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A ferroelectric thin-film transistor (FeTFT)-based synaptic device with an indium–gallium–zinc oxide (IGZO) channel and a metal–ferroelectric–metal–insulator–semiconductor (MFMIS) structure is reported. The fabricated FeTFT exhibits a highly linear conductance response ($|\alpha| = 0.21$) with a large dynamic range ($G_{\max}/G_{\min} \approx 53.2$), although identical program pulses are applied to the device. In addition, because the inner metal layer of the FeTFTs has an MFMIS structure, the electric field is uniformly applied to the entire IGZO channel, which reduces the cycle-to-cycle variation ($\sigma = 0.47\%$) in the conductance responses. In the system simulation with the measured synaptic characteristics, the high classification accuracy of $\approx 97.0\%$ is achieved in the MNIST image set, verifying the feasibility of FeTFT-based neuromorphic systems.

1. Introduction

Neuromorphic computing using analog synaptic devices has been actively studied as a new computing paradigm to replace von Neumann computing architectures.^[1–5] Because data communications are significantly eliminated in brain-inspired neuromorphic systems according to Kirchhoff's current law, the energy consumption and system latency are significantly lowered, improving the computation efficiency.^[6–9] From this perspective, many artificial synaptic devices have been reported for neuromorphic computing applications, such as resistive random access memory

(ReRAM),^[10–14] flash devices,^[15–20] and ferroelectric-based devices.^[21–25] These analog synaptic devices have the advantages of multilevel weight storage, nonvolatile memory function, and high density compared to digital memory (e.g., static random access memory). Among the various synaptic devices, ferroelectric field-effect transistors (FeFETs) have attracted more interest as one of the promising candidates, owing to their compatibility with complementary metal-oxide-semiconductor (CMOS) process technology, low fabrication temperature, and low operation voltage.^[26–34]

Despite their promising potential, many FeFET-based synaptic devices suffer from nonideal synaptic characteristics, including nonlinearity, low dynamic range, and device variation. These nonideal characteristics can cause errors in vector matrix multiplications (VMMs) and weight updates, thereby degrading the accuracy of neuromorphic systems.^[35–39] Many studies have reported strategies to mitigate the nonidealities of FeFET-based synaptic devices. For example, incremental-step-pulse programming (ISPP) methods have been used to obtain linear conductance responses in FeFET-based synaptic devices.^[30,31,40–42] Iterative write-read-verify programming methods have also been widely used to address device variations.^[43] However, these methods require additional circuitries and memory to generate programming pulses with different amplitudes or to read the conductance of the devices during the verification process.^[38,44,45] Thus, the area and energy consumption of neuromorphic systems can be significantly increased by adopting the methods. For high accuracy and efficiency of FeFET-based

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neuromorphic systems, artificial synaptic devices exhibiting excellent synaptic characteristics should be developed.

Here, we report a ferroelectric thin-film transistor (FeTFT)-based synaptic device with an indium–gallium–zinc oxide (IGZO) channel and a metal–ferroelectric–metal–insulator–semiconductor (MF MIS) gate structure. Because the FeTFT with an MF MIS structure exhibits a large memory window (MW) due to the capacitance matching between the gate stack,^[46–48] the device has a large dynamic range. In addition, the device exhibits highly linear conductance responses to identical pulses, reducing the hardware burden of obtaining linear weight updates. We also demonstrated that the fabricated FeTFT has a significantly low cycle-to-cycle (C2C) variation in the repeated potentiation curves. Finally, we evaluated the accuracy of the on-chip training of hardware neural networks for image classification using the synaptic characteristics of the FeTFTs. These results verify the high performance of FeTFT-based synaptic devices in neuromorphic systems and provide insights into obtaining superior synaptic characteristics.

2. Results and Discussion

2.1. Electrical Characteristics of the FeTFTs

A 3D schematic view of the FeTFT with an MF MIS structure and its cut view between the source and drain are shown in Figure 1a, b, respectively. The transmission electron microscope (TEM) image are shown in Figure 1c. As a channel layer, the FeTFT has an IGZO material that can be deposited at a lower fabrication temperature than the annealing temperature to exhibit ferroelectricity in the HZO layer. Furthermore, the TFTs with the IGZO channel show a high on/off current ratio,^[49] which is advantageous in obtaining a large dynamic range. In the FeTFT

with an MF MIS structure, the area ratio (AR) between the metal–insulator–semiconductor (MIS, A_{MOS}) and the metal–ferroelectric–metal (MFM, A_{FE}) can be flexibly engineered. Accordingly, the capacitance ratio of the MIS and the MFM layers in the MF MIS structure can be modulated by the ratio of A_{MOS} and A_{FE} . This indicates that the electric field across the MFM layer can be increased by increasing the AR ($A_{\text{MOS}} : A_{\text{FE}}$), maximizing the polarization in the ferroelectric material and improving the MW of the FeTFTs with the MF MIS structure. In addition, proper capacitance matching between the layers enhances the reliability of the devices by reducing the electric field across the dielectric.^[32,48,50–52] Figure 1d shows the current versus voltage at different voltage sweep ranges in the MFM structure, obtained through positive-up-negative-down (PUND) measurements at a frequency of 100 kHz. Figure 1e shows the polarization versus voltages at different voltage sweep ranges in the PUND measurements, showing a remnant polarization ($2P_r$) of $\approx 46 \mu\text{C cm}^{-2}$. The capacitance versus voltage curves as a parameter of voltage sweep range are shown in Figure S1, Supporting Information. The electron-dispersive spectrometer (EDS) mapping is shown in Figure S2, Supporting Information.

Figure 2a shows the double-sweep I_D – V_{GS} curves at different sweep ranges in the fabricated FeTFT with an AR of 7:1, exhibiting an anticlockwise hysteresis loop resulting from the polarization in the HZO layer. The MW at a constant current level of 40 nA was ≈ 3.8 V. The channel width and length were 30 and 20 μm , respectively. We investigated the MW of the FeTFTs as a parameter of the AR (Figure 2b, linear scale curves in Figure S3, Supporting Information). Because the capacitance of the MFM layer decreased as the AR increased at the same A_{MOS} , the electric field across the MFM ratio also increased as the AR increased. Thus, the FeTFT can utilize the fully saturated

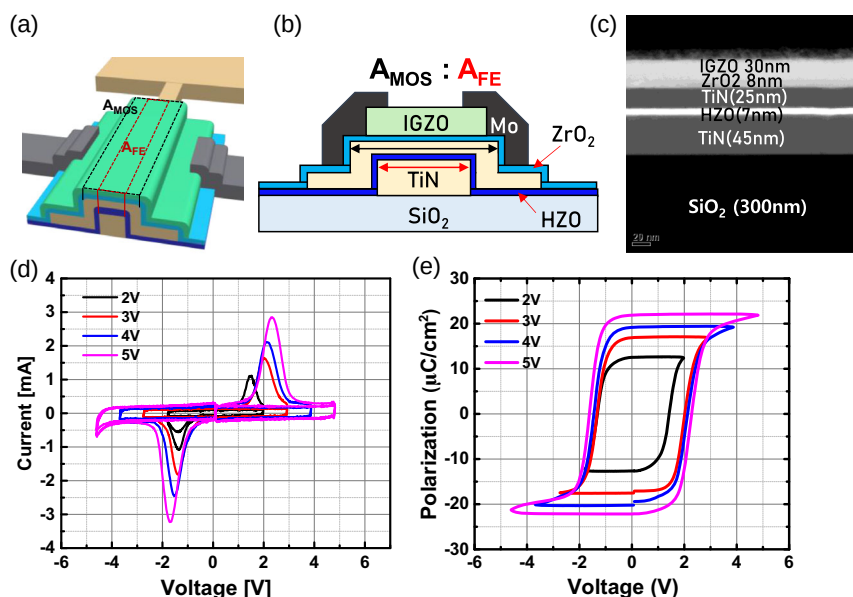


Figure 1. a) 3D schematic view of the FeTFT schematic diagram of the FeTFT with an MF MIS structure and b) cut view between the source and drain. c) TEM image of the gate stack of the FeTFT. d) Current versus voltage curves in the MFM structure as a parameter of voltage sweep range. e) Polarization versus voltage curves in the MFM structure as a parameter of voltage sweep range.

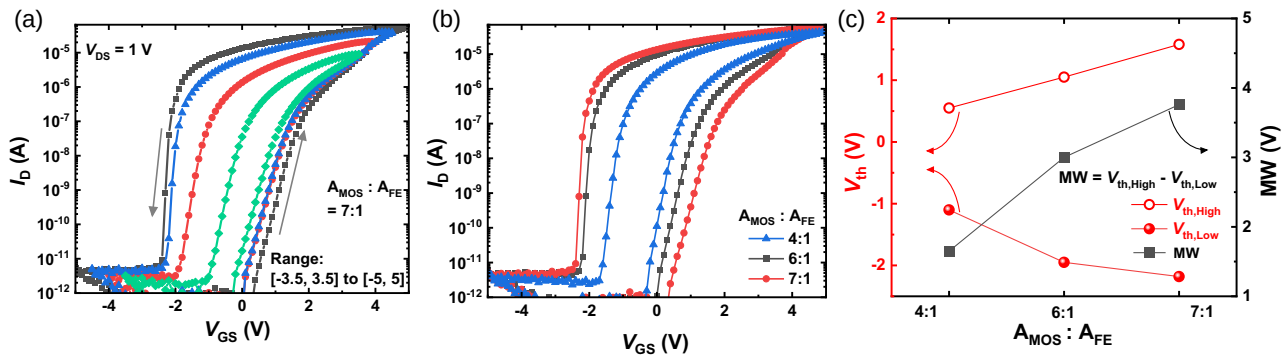


Figure 2. a) Double-sweep I_D - V_{GS} curves of the FeTFTs with different sweep ranges at a V_{DS} of 1 V. The AR is 7:1. b) Double-sweep I_D - V_{GS} curves of the FeTFTs at a V_{DS} of 1 V as a parameter of the AR. c) V_{th} and MW versus the AR. Red circle symbols indicate the V_{th} s, and black square symbols indicate the MW.

polarizations of the MFM layer, maximizing the MW.^[51] The threshold voltages (V_{th} s) and MWs of the FeTFTs are shown in Figure 2c.

2.2. Synaptic Characteristics of the FeTFTs

The fabricated FeTFT with an MFMIS gate stack can be used as a synaptic device by modulating the channel conductance (G),

which is used to determine the synaptic weight in neuromorphic systems. The changes in G were implemented through polarization switching of the HZO layer, in which multiple domains exist. Figure 3a shows the I_D - V_{GS} curves of the FeTFT with an increasing number of program pulses (PGM, 5 V, 100 μ s). Before the PGM pulses, the FeTFT was initialized using ten erase pulses (ERS, -5 V, 10 ms). After ERS pulses were applied to the device, downward polarization was set in the HZO layer, depleting the electrons in the IGZO channel and decreasing G of the

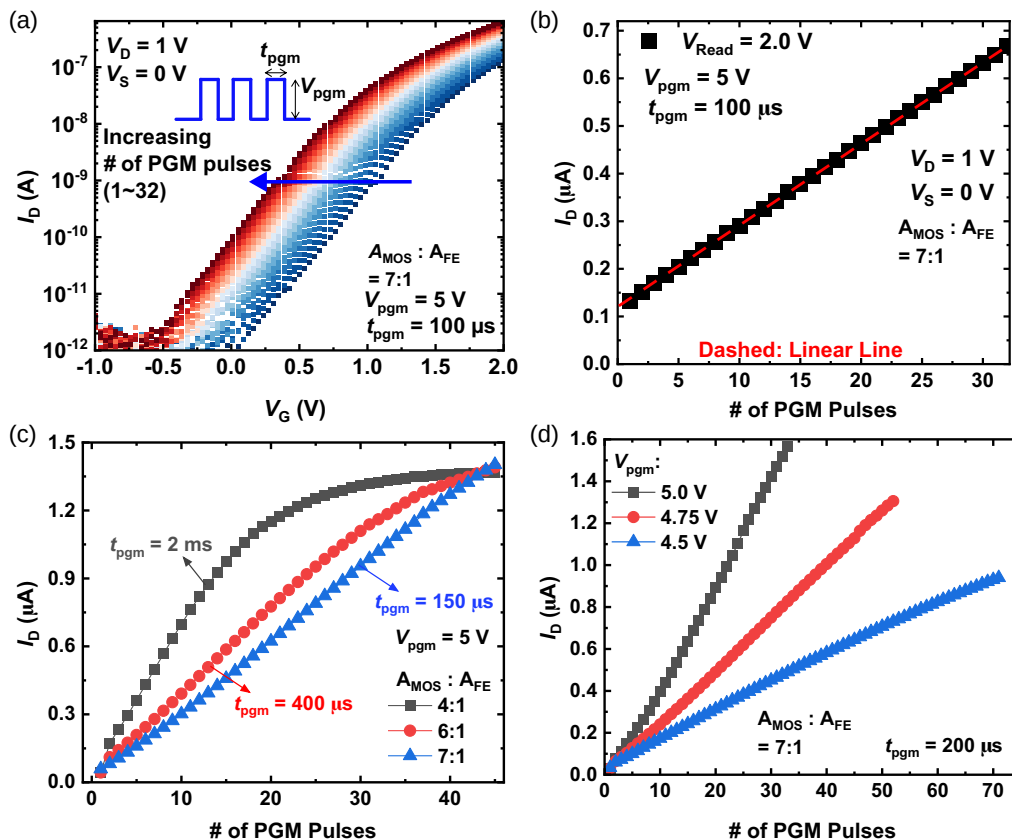


Figure 3. a) Transfer curves of FeTFTs with increasing the number of PGM pulses. b) Conductance response to the PGM pulses at a read voltage of 2 V. c) Conductance responses of FeTFTs with different ARs within the same dynamic range. d) Conductance responses of the FeTFT as a parameter of PGM pulse amplitude.

FeTFT. In contrast, the PGM pulses changed the polarization direction upward, accumulating electrons in the channel and increasing G of the FeTFTs. In addition, the gradual increase in G was observed in the FeTFTs.^[41,53] Figure 3b shows the G response of the FeTFT with the number of PGM pulses. Interestingly, the G response of the FeTFT was linear with the number of PGM pulses, although the applied PGM pulses were identical. Many works reported the ISPP scheme to mitigate nonlinear G responses in various FeFET-based synaptic devices.^[30,31,40–42] However, it is worth noting that generating incremental PGM pulses requires additional circuits and degrades the efficiency of neuromorphic systems.^[44] From this perspective, the highly linear G response in the fabricated FeTFTs with the identical PGM pulses is a significant advantage in neuromorphic systems. According to a previously reported model,^[53] the measured linearity of the FeTFT was -0.72 . A comparison of G responses to PGM and ERS pulses is shown in Figure S4, Supporting Information. Some charge-trapping FET-type synaptic devices have been reported with highly linear G responses in the subthreshold operating region.^[54] However, because the subthreshold current of FETs is highly sensitive to voltage changes, neuromorphic systems with FET-type synaptic devices can be degraded by external noise or voltage fluctuations. In contrast, the fabricated FeTFTs with the MFIS structure exhibited a highly linear G response above the subthreshold region, enhancing the latency and reliability of neuromorphic systems.

Additionally, we analyzed the G responses of the FeTFTs with different ARs. As shown in Figure 3c, the FeTFT with an AR of 7:1 had a more linear G response within the same dynamic range ($G_{\max}/G_{\min}$) than the others. Although the FeTFTs with ARs of 4:1 and 6:1 also exhibited linear G responses within the narrower dynamic range (Figure S5, Supporting Information), the FeTFT with an AR of 7:1 exhibited linearity with a wider dynamic range. Figures S6 and S7, Supporting Information, show G responses of the FeTFTs with different ARs at the same t_{pgm} s and those with an AR of 7:1 at different t_{pgm} s, respectively. To investigate the linearity, we compared the I_D – V_{GS} curves of the FeTFTs with different ARs and V_{th} changes by PGM pulses (Figure S8, Supporting Information) under the PGM condition shown in Figure 3c. Figures S8a, Supporting Information, shows the normalized I_D – V_{GS} curves of the FeTFTs with different ARs, in which the V_{th} s of the FeTFTs were set to the same value.

The normalized I_D – V_{GS} curves were almost identical among the FeTFTs with different ARs. We also investigated the ΔV_{th} as a function of the PGM pulse number, as shown in Figure S8b, Supporting Information. By applying PGM pulses to the gate of the FeTFT, the I_D – V_{GS} curve was parallelly shifted to the left by ΔV_{th} , leading to corresponding changes in the I_D of the FeTFT. Note that if the changes in I_D by ΔV_{th} and the ΔV_{th} by PGM pulses cancel each other, the I_D linearly increases with the number of PGM pulses, resulting in a linear G response. From this perspective, we can engineer the AR of FeTFTs to overlap the black and red symbols within the given dynamic range (Figure S8c, Supporting Information). The ΔV_{th} quickly saturates with the PGM pulses in the FeTFT with an AR of 4:1 due to the narrow MW, whereas the saturation value of ΔV_{th} increased as the AR increased. As a result, the black and red symbols overlap each other in the FeTFT with an AR of 7:1 for the given dynamic range, and we can observe a highly linear G response. Figure 3d shows G responses as a parameter of the PGM pulse amplitude at a pulse width of 200 μs . The responses exhibited high linearity with different pulse amplitudes. The dynamic range at a PGM voltage of 5 V was ≈ 53.2 , which was higher than that of other ferroelectric-based synaptic devices.^[26,28,40,41,53] In addition, the FeTFT exhibited more than 70 weight levels with a high linearity at a PGM voltage of 4.5 V. The fitting results for each G response obtained using the reported model^[53] are shown in Figure S9, Supporting Information. The retention characteristics of the fabricated FeTFTs are shown in Figure S10, Supporting Information, indicating that nonvolatile memory function is implemented in the FeTFTs.

FeFETs with an MFIS structure suffer from inhomogeneous polarization, which can lead to nonuniform channel conductivity and variation in the G responses. In contrast, the main advantage of the FeTFTs with an MFIS structure is that the inserted metal layer rectifies the inhomogeneous polarization in the ferroelectric layer^[55] (Figure 4a). Thus, the electric field through the inserted metal layer is uniformly applied to the entire channel, resulting in uniform conductivity of the channel and reduction of the C2C variation. Figure 4b shows five repeated G responses of the FeTFT to identical PGM pulses to evaluate C2C variation. Each G response was measured after initializing the G level using 20 ERS pulses. As shown in Figure 4b, almost the same G responses were obtained with a low C2C variation

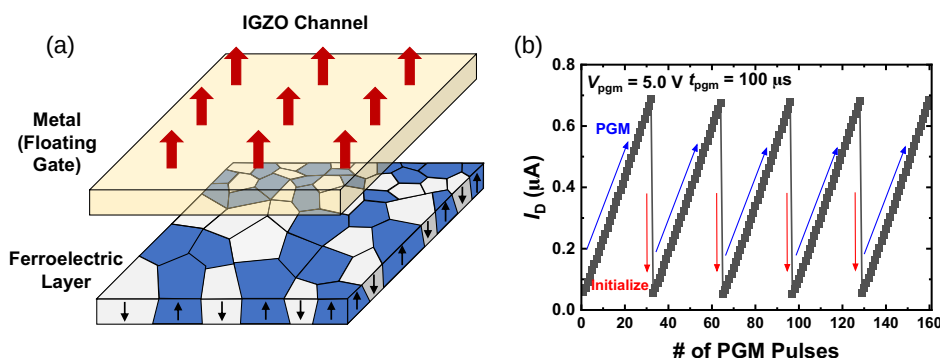


Figure 4. a) Schematic diagram of HZO layer and the inserted metal layer. The electric field can be uniformly applied to the IGZO channel through the inserted metal layer. b) Five repetitions of G responses of the FeTFT with an AR of 7:1.

($\sigma = 0.47\%$, Figure S11, Supporting Information) while exhibiting high linearity. We also measured C2C variation of four more FeTFTs, as shown in Figure S12, Supporting Information, verifying the low C2C variation in multiple devices. In addition, no write-read-verify process was used to mitigate the C2C variation of the FeTFTs, indicating that the hardware for the process is not necessary if the FeTFTs are used in neuromorphic systems. Note that the C2C variation in synaptic devices significantly degrades the accuracy of neuromorphic systems and should be reduced.^[35,36] Thus, the low C2C variation is an important advantage of the FeTFT with an MFMS structure as a synaptic device.

2.3. Network Simulation

In order to evaluate on-chip training performance using the FeTFTs, we designed a two-layer fully connected neural network for MNIST image classification with a size of 784-256-10, as shown in Figure 5a. Two FeTFTs represented a weight value (W): $W = G_+ - G_-$, where G_+ and G_- are the conductance of FeTFTs to represent positive and negative weights, respectively (Figure 5b). Each G value of the FeTFTs was modulated by the ferroelectric polarization state in the HZO layer. The current mirror circuit can perform a subtraction between the current from the G_+ array and the current from the G_- array. Then, the resulting subtracted current can be converted into a pulse-width signal in a pulse-width modulation circuit.^[56] The network training was simulated in the PyTorch framework considering the linearity of the G response, weight precision (conductance levels), C2C variation, and dynamic range, which were measured in the fabricated FeTFTs. To fully utilize the linear G responses in FeTFTs, we adopted the Manhattan weight update rule, in which weight updates can be performed using only the potentiation part of

the synaptic devices.^[39] Figure 5c shows an example of weight updates in this scheme. When ΔW was zero, no PGM pulse was applied to either FeTFTs. When ΔW was larger than update threshold (Δ_{th}) (smaller than $-\Delta_{th}$), one PGM pulse was applied to the FeTFT representing a positive (negative) weight. Subsequently, the weight was updated one step by the single PGM pulse. During the training process, either of the two FeTFTs could have the maximum G and be stuck, making the weight update unidirectional. In this case, both FeTFTs were initialized first by the ERS pulses, and then the PGM pulses were applied to the FeTFT with the maximum G until the weight reached the previous value. Subsequently, the weight could be updated bidirectionally using the device pair without being stuck. An example of G updates in the FeTFTs is shown in Figure S13, Supporting Information, during the training process. Through this scheme, the weight updates were performed linearly and symmetrically using the potentiation part of the synaptic devices, thereby increasing the accuracy. In addition, the hardware burden of generating incremental PGM/ERS pulses was reduced, mitigating the power and area overhead of the systems. A more detailed description is represented in Experimental Section.

The classification accuracy versus the training epoch was evaluated using the device characteristics (Figure 5d). The network achieved a high accuracy of $\approx 96.3\%$ under the measured PGM conditions. In particular, an accuracy of $>97.0\%$ was achieved at a PGM pulse amplitude of 4.5 V. Although the accuracy achieved in Pytorch can be further degraded in SPICE simulation where parasitic capacitance and resistance are calculated additionally, these results still demonstrated that the synaptic characteristics of the fabricated FeTFTs are highly effective for training neuromorphic systems. The impact of device nonidealities on the classification accuracy is shown in Figure S14, Supporting

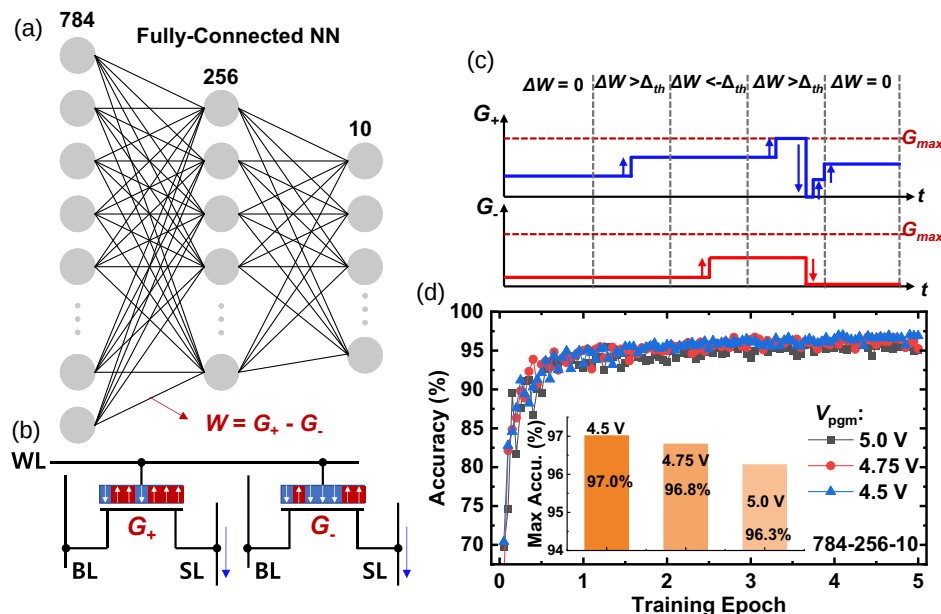


Figure 5. a) Fully connected neural network with a size of 784-256-10. b) Synaptic weight consisting of two FeTFTs. c) Example of weight update rule using only potentiation parts of the FeTFTs in the synaptic weight. When the G_+ of FeTFT reaches the G_{max} , both FeTFTs are erased, and then the FeTFT for G_+ is programmed until the weight reaches the previous value. d) Accuracy curve as a parameter of PGM pulse amplitude. (Inset) Maximum accuracy with the pulse amplitude.

Information. A comparison of the synaptic characteristics with those of other ferroelectric-based synaptic devices is presented in Table S1, Supporting Information. The fabricated FeTFTs with an MFMS structure exhibited superior synaptic characteristics for high-performance neuromorphic systems, including high linearity with identical pulses, multilevel weight precision, high dynamic range, and low C2C variation.

3. Conclusion

We fabricated FeTFTs with an IGZO conductive channel and MFMS structure and investigated their synaptic characteristics for neuromorphic systems. Due to the MFMS structure that can fully utilize the polarization loop of the ferroelectric layer, the FeTFT exhibited a highly linear G response ($|\alpha| = 0.21$) with a high dynamic range ($G_{\max}/G_{\min} \approx 53.2$). Moreover, the inserted metal layer rectifies the inhomogeneous electric field, resulting in low C2C variation ($\sigma = 0.47\%$). We also evaluated the performance of on-chip training using the synaptic characteristics of the fabricated FeTFTs, and high classification accuracy was achieved (97.0%). These results verify the feasibility of high-performance FeTFT-based neuromorphic systems and provide insights into obtaining superior synaptic characteristics of artificial synapses.

4. Experimental Section

Fabrication of FeTFT with an MFMS Structure: Figure S15, Supporting Information shows the key fabrication steps. First, TiN as a bottom gate was deposited and patterned on a buffered oxide at a thickness of 45 nm. Subsequently, hafnium zirconium oxide (HZO, 8 nm) was deposited as a ferroelectric layer, and TiN (25 nm) was deposited and patterned as a floating gate. The AR between the bottom and the floating gates can be engineered to modulate the electric field across the HZO layer. After thermal annealing at 500 °C for 30 s to induce the ferroelectricity in the HZO layer (N_2 condition), ZrO_2 (8 nm) was deposited as a dielectric layer. Next, amorphous IGZO was deposited as a channel layer using radio frequency (RF) sputtering and patterned. After annealing the IGZO channel at 350 °C for 1 h (O_2 condition), Mo was deposited by DC sputtering to form a source/drain.

Characterization: The characteristics of the fabricated FeTFTs were measured and investigated using a semiconductor parameter analyzer (Agilent, B1500a) at room temperature. Simulations of hardware-based neuromorphic systems were conducted using the PyTorch framework, which was widely used for deep neural network simulations.

Network Simulation: The network simulation was conducted in the PyTorch framework using the measured characteristics of the FeTFTs. The fully connected neural network with a size of 784-256-10 was designed for MNIST image classification. The batch size of the training was 100. The activation function of the hidden layer was rectified linear unit (ReLU) function, and that of the output layer was softmax function for cross-entropy loss function. The activated value in the layer ($l \in \{1, 2\}$), X^l , was represented as follows

$$X^l = f(X^{l-1}(G_+^l - G_-^l)) \quad (1)$$

where f is the activation function, and G^l is the conductance of FeTFTs. X^0 represents the matrix in the input layer. Here, the maximum conductance was set to value of 1 for simplicity. In the output layer ($l = 2$), the cross-entropy loss and the delta value in the output layer (δ^2) were obtained with the X^2 and the true labels. The delta value in the hidden layer (δ^1) was represented as follows

$$\delta^1 = \delta^2(G_+^2 - G_-^2)^T \cdot f' \quad (2)$$

where f' was the derivative of the ReLU activation function in the hidden layer. According to (1) and (2), the amount of weight update in the layer l (ΔW) was calculated as follows

$$\Delta W^l = \gamma(X^{l-1})^T \delta^l \quad (3)$$

where γ was the learning rate of the training process and set to a value of 1. Subsequently, one PGM pulse was applied to the FeTFT for the positive weight if $\Delta W > \Delta_{th}$, while one PGM pulse was applied to the FeTFT for the negative weight if $\Delta W < -\Delta_{th}$. The update threshold, Δ_{th} , was set to a value of 0.05. Through this training scheme, we assumed that the conductance of FeTFTs was updated by the PGM pulses along the response, which led to weight updates in hardware-based neuromorphic systems.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Dongseok Kwon contributed in data curation; formal analysis; writing the original draft. E.C.P. contributed in conceptualization and formal analysis. W.S. contributed in formal analysis. R.-H.K. contributed in formal analysis. J.-H.B. contributed in review and editing. Daewoong Kwon contributed in funding acquisition; resources; supervision; and writing the review and editing. J.-H.L. contributed in funding acquisition; resources; supervision; and writing the review and editing.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

ferroelectric, ferroelectric thin-film transistors, indium–gallium–zinc oxide, metal–ferroelectric–metal–insulator–semiconductor, neuromorphic systems, synapses

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