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Ultrafast intense pulsed light bonding process for multi-die stacked packages

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ABSTRACT

In this study, we report the first demonstration of the intense pulsed light (IPL) flip-chip bonding process for multi-die stacked package assemblies (2-, 3-, and 4-die configurations). While conventional methods struggle with thermal management in 3D stacks, this work demonstrates that the IPL process inherently produces a top-down temperature and time above liquidus (TAL) gradient, optimized at 50, 70, and 110 pulses for each respective configuration via FEM simulation. The resulting intermetallic compound (IMC) thickness (0.7–2.0 μm) exhibited a precise layer-by-layer gradient consistent with the predicted thermal distribution. The IPL process completed bonding within 0.5–1.1 s, achieving 29–78 % thinner IMC layers and fewer interfacial defects compared to conventional mass reflow. Thermal cycling tests revealed that IPL-bonded packages sustained 1.9–4.7 times more cycles to failure than their reflow counterparts. Notably, the transition from interface failure to solder crack failure in the 2-die package underscores that reduced thermal exposure preserves interfacial integrity. These results demonstrate that the IPL bonding process is a viable high-speed alternative for 3D multi-die packaging, offering improved microstructural control and enhanced thermomechanical reliability compared to mass reflow.

1. Introduction

The semiconductor industry has been constantly demanding higher performance, lower power consumption, and smaller sizes of semiconductor devices [1,2]. As the physical limits of conventional scaling are reached, three-dimensional (3D) integrated circuits (ICs), which stack multiple semiconductor chips vertically, have attracted significant attention for reducing interconnect length and enabling heterogeneous integration [3,4]. In particular, high-bandwidth memory (HBM) has emerged as a critical component for artificial intelligence (AI) and high-performance computing (HPC) applications, driving the need for reliable and scalable multi-die bonding technologies [5,6]. The development and optimization of interconnection technologies are therefore essential for the advancement of 3D semiconductor package integration.

For multi-die stacking, several bonding technologies have been developed. Thermocompression bonding (TCB) with non-conductive film (NCF) has been widely used for its precise alignment and low thermal stress, but its sequential chip-by-chip processing limits productivity as the number of stacked layers increases [7–9]. In addition, the TCB process typically requires heating the die above 300 °C under applied pressure, which can induce thermal damage to the package components [10]. To overcome this throughput limitation, the mass reflow with molded underfill (MR-MUF) process has been adopted in industrial HBM production, enabling simultaneous bonding of all die layers in a single reflow step with improved thermal dissipation compared to TC-NCF [6,11]. However, as the number of stacked layers continues to increase, minimizing the peak temperature and time above liquidus during the bonding process becomes increasingly important for controlling IMC growth and preserving joint integrity across all interconnection layers [12]. The conventional reflow thermal profile, with a typical peak temperature of 220–260 °C and time above liquidus (TAL) of 30–120 s [13], can result in excessive IMC growth at solder interfaces, which exhibits brittle characteristics and increases the risk of fracture under thermomechanical stress [14–16]. Laser-assisted bonding (LAB) has also been explored for 3D chip stacking, with Bragança *et al.* [17] demonstrating collective bonding of up to six TSV dies using a high-power laser. However, LAB throughput remains limited by the small bonding area and sequential or small-batch nature of laser processing,

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making it challenging to scale for high-volume multi-die production.

As an alternative energy source for ultrafast bonding, intense pulsed light (IPL) has been proposed. IPL utilizes broadband light (350–950 nm) from a xenon lamp to deliver high-density radiant energy in extremely short pulse durations (millisecond-scale). This photothermal mechanism enables localized heating from the top die surface with extremely short process times, minimizing the overall thermal exposure to the package, as we demonstrated in our previous single-chip study [18]. Previous studies have demonstrated the effectiveness of IPL soldering for single-chip packages: Jang et al. investigated IPL soldering on OSP and ENEPIG surface-finished substrates with enhanced mechanical properties [19]; Ha et al. examined the drop impact reliability of IPL-soldered joints [20]; and Min et al. successfully implemented low-power IPL soldering for ball grid array (BGA) packages [21]. In our prior work, we developed an IPL flip-chip bonding process for single-chip FC-BGA packages, demonstrating a reduction in IMC thickness from 6 μm to approximately 800 nm, a process time reduction from 90 s to 56.4 ms, and a 30% improvement in die shear force compared to the conventional reflow process [18]. However, the extension of IPL bonding technology to multi-die stacked configurations has not been explored.

In a novel advancement, in this work, the IPL flip-chip bonding process is implemented in multi-die stacked packaging, comprehensively covering 2-die to 4-die assemblies. A validated finite element method (FEM) thermal simulation model is employed to predict the temperature distribution across each interconnection layer and to determine the optimal IPL process parameters. The microstructural characteristics at each interconnection layer are systematically investigated and compared with those of the conventional mass reflow process. Furthermore, thermal cycling reliability tests with in-situ resistance monitoring are conducted to evaluate the thermomechanical reliability of the IPL-bonded multi-die packages.

2. Experimental section

2.1. Multi-die Stacked Package Specimens

Fig. 1 shows the schematic configuration of the multi-die stacked package specimens used in this study. The specimen structure was designed based on the single-flip chip package from our previous work [18], with modifications to incorporate through-silicon via (TSV) interconnects and multi-die stacking capability. As shown in Fig. 1(a), the generalized n-die stacked package consists of a top die, middle dies, and a base die. The top die (Fig. 1(a-1)) consists of Cu bridges (10 μm thick) for daisy chain routing and Cu posts (40 μm thick) with Sn-3.5Ag solder caps (20 μm thick). The middle dies (Fig. 1(a-2)) incorporate TSVs (80 μm diameter) with Cu pads (10 μm thick) on the top side and have the same bump structures as the top die on the bottom side, but without Cu bridges. The base die (Fig. 1(a-3)) also incorporates TSVs structure with Cu pads on the top side, while the bottom side features under-bump metallization (UBM; Cu 10 μm /Ni 3 μm/Au 0.05 μm thick) and SAC305 solder balls (300 μm diameter) for interconnection with a printed circuit board (PCB) substrate. The cross-sectional SEM images of each die level are provided in the Supporting Information (Fig. S1). All dies were silicon wafers diced to 10 mm × 10 mm. The ball grid array consists of 36 I/O connections arranged in a 6 × 6 array with a 1.0 mm pitch. Organic solderability preservative (OSP)-coated PCB substrates (14 mm × 14 mm × 1 mm) with matching 36 I/O connections were used (Fig. 1(b)). Fig. 1(c-d) show the optical images of the top die with Cu posts with Sn-3.5Ag caps and the base die with SAC305 solder balls, respectively. As shown in Fig. 1(c), the daisy chain routing consists of three independent lines, denoted as the outer, middle, and inner lines,

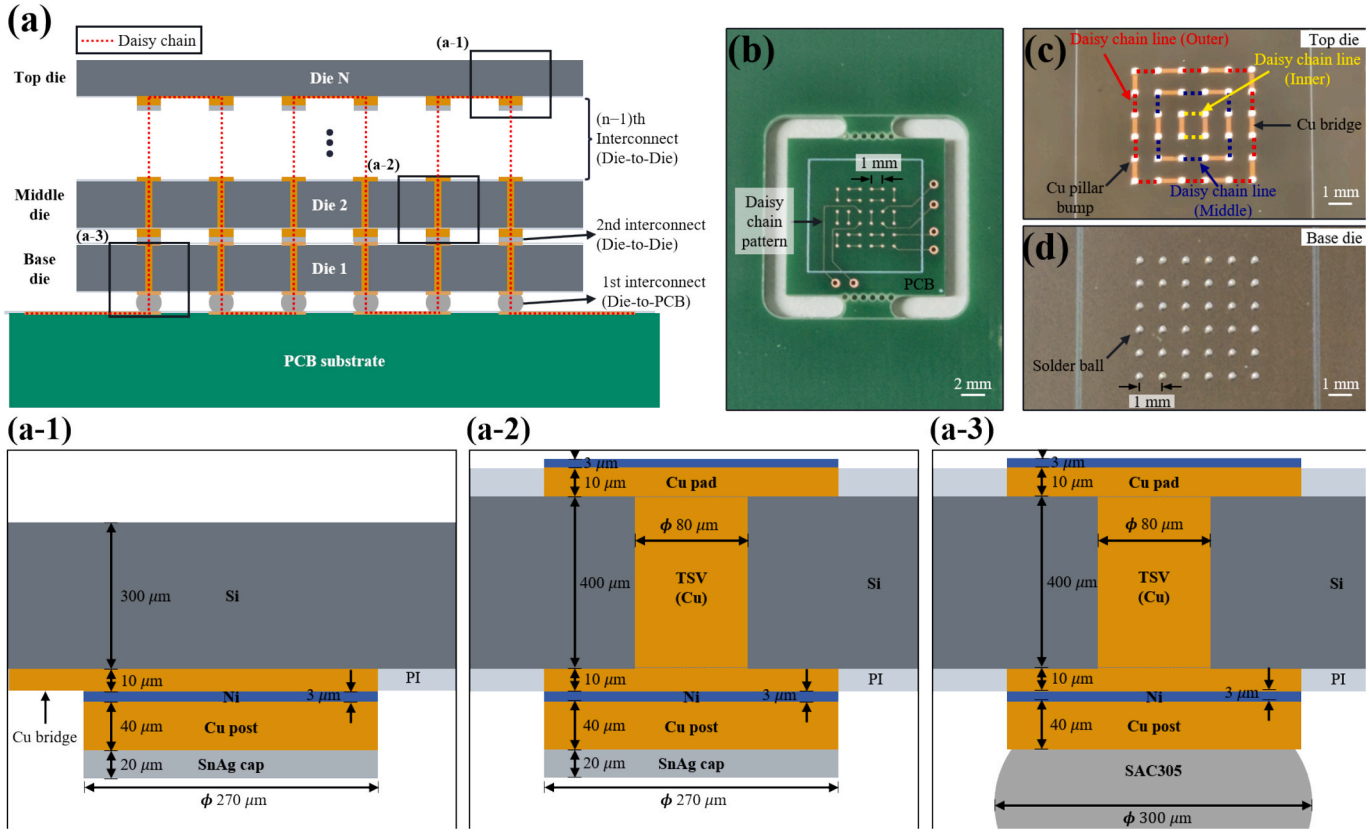

Fig. 1. Schematic configuration of the multi-die stacked package specimen. (a) Cross-sectional view of a generalized n-die stacked package with Cu pillar bump interconnections and daisy chain pattern for in-situ resistance monitoring. Enlarged views show the interconnection structures of (a-1) the Top die, (a-2) the middle die, and (a-3) the base die. (b) Optical image of the PCB substrate with daisy chain routing. (c) Top die with Cu pillar bumps. (d) Base die with SAC305 solder balls.

which cover different regions of the die area. Each line is routed vertically through the entire stack and connects the corresponding interconnections of all layers in series, so that a single unbonded interconnect anywhere along a line results in an open circuit. Electrical continuity of a given line therefore confirms that all interconnections belonging to that line were successfully bonded across all interconnection layers.

2.2. Bonding Processes

The IPL system consisted of a xenon lamp (wavelength: 350–950 nm; PerkinElmer Co.), reflector, pulse controller, power supply, water-cooling system, and a height-adjustable lamp housing that enables fine control of the distance between the lamp and the specimen. Before the bonding process, flux (WF-6317, Senju Metal Industry) was applied to all solder surfaces, including the SAC305 solder balls on the base die and the Sn-3.5Ag solder caps on the middle and top dies. For the simultaneous bonding approach, all dies were pre-stacked and aligned before IPL irradiation (see Fig. 2(a)). The IPL parameters were fixed at 1.5 ms pulse on-time and 100 Hz frequency, and the irradiation energy per pulse was fixed at 1.4 J/cm^2 (power supply voltage: 1100 V), consistent with the optimized conditions from our single-chip study [18]. Using the height-adjustable housing, the distance between lamp housing exit and the top chip surface was fixed at 10 mm for all configurations, and the incident energy density at the top chip surface was measured with an energy meter (Nova, Ophir Optronics Solutions Ltd.) to ensure identical irradiation energy across all multi-die specimens regardless of stack height. Fig. 2(b–d) show the schematic configurations of the 2-, 3-, and 4-die stacked packages, and Table 1 summarizes the optimized IPL irradiation conditions, determined from the FEM thermal simulation (50 pulses for 2-die, 70 pulses for 3-die, and 110 pulses for 4-die stacked packages). For comparison, multi-die stacked packages were also assembled using a conventional mass reflow process. All dies were pre-stacked and aligned, and then bonded simultaneously in a single reflow cycle. The reflow soldering process was performed using a reflow machine (GF-B-HT, Novastar) with a peak temperature of 250 °C and a total reflow zone duration of approximately 5 min. The detailed reflow temperature profile is provided in the Supporting Information (Fig. S2). Both the IPL and mass reflow processes were performed in air using the same flux.

Table 1
IPL irradiation conditions for multi-die stacked packages.

PKG	On-time (ms)	Frequency (Hz)	Pulse number (counts)	Irradiation energy (J/cm^2)
2-die stacked PKG	1.5	100	50	1.4
3-die stacked PKG	1.5	100	70	1.4
4-die stacked PKG	1.5	100	110	1.4

Note: On-time, frequency, and irradiation energy per pulse were determined based on the optimized conditions from the previous study [18].

2.3. Finite Element Method Simulation

The FEM thermal transient simulation model, which was established and validated through in-situ temperature monitoring using a K-type thermocouple in our previous single-chip study [18], was extended to the multi-die stacked configurations using the ABAQUS program (SIMULIA). Three-dimensional models were developed for 2-die, 3-die, and 4-die configurations, as shown in Fig. 3(a). The models included silicon dies (Si; 300 μm thick for the top die and 400 μm thick for the middle/base dies), Cu posts (Cu; 40 μm thick), Sn-3.5Ag bumps (Sn-3.5Ag; 20 μm thick), solder balls (SAC305; 300 μm diameter), polyimide passivation layer (PI; 10 μm thick), photosensitive solder resist (PSR; 30

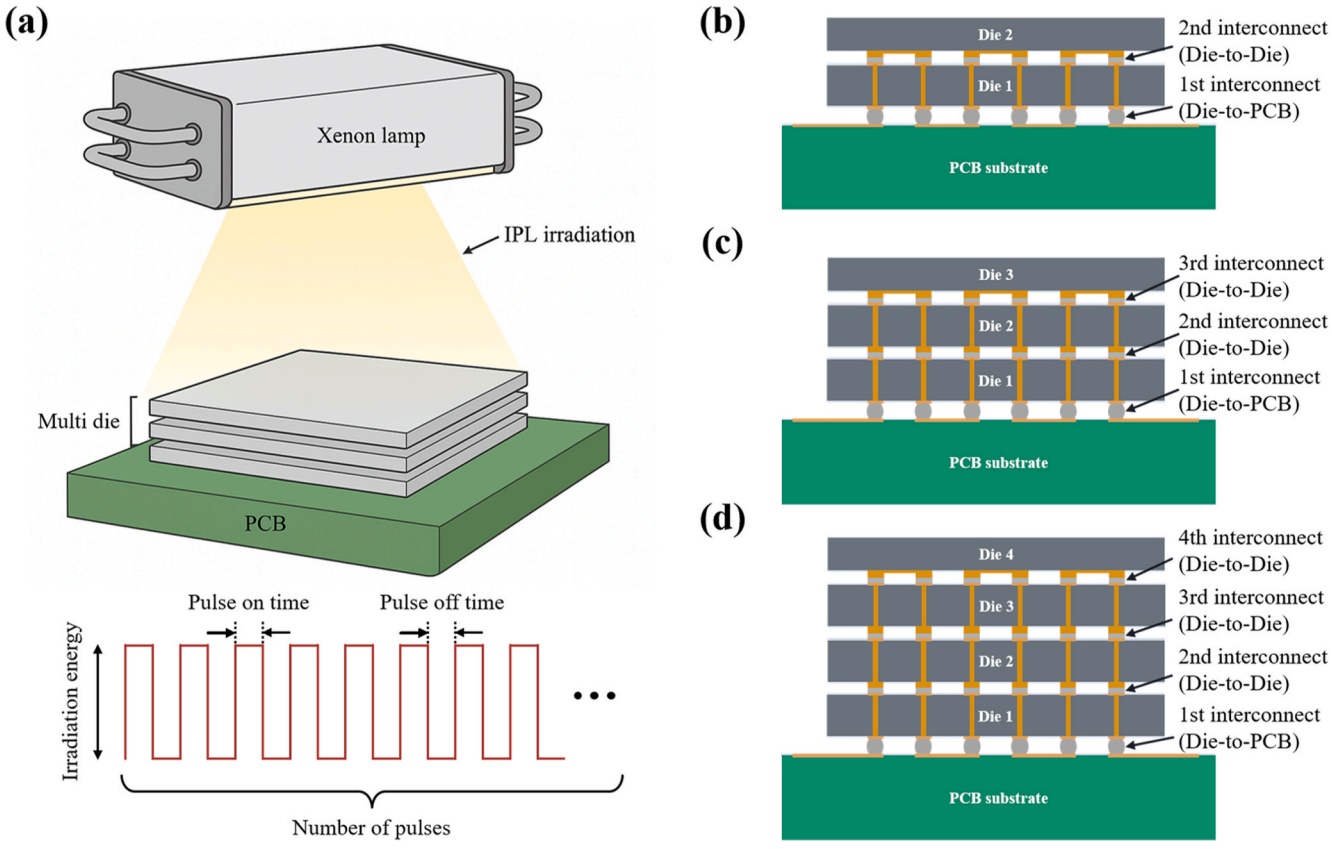

Fig. 2. (a) Three-dimensional illustration of the simultaneous IPL flip-chip bonding process on a multi-die stacked package with IPL irradiation parameters. Schematic cross-sectional configurations of (b) 2-die, (c) 3-die, and (d) 4-die stacked packages.

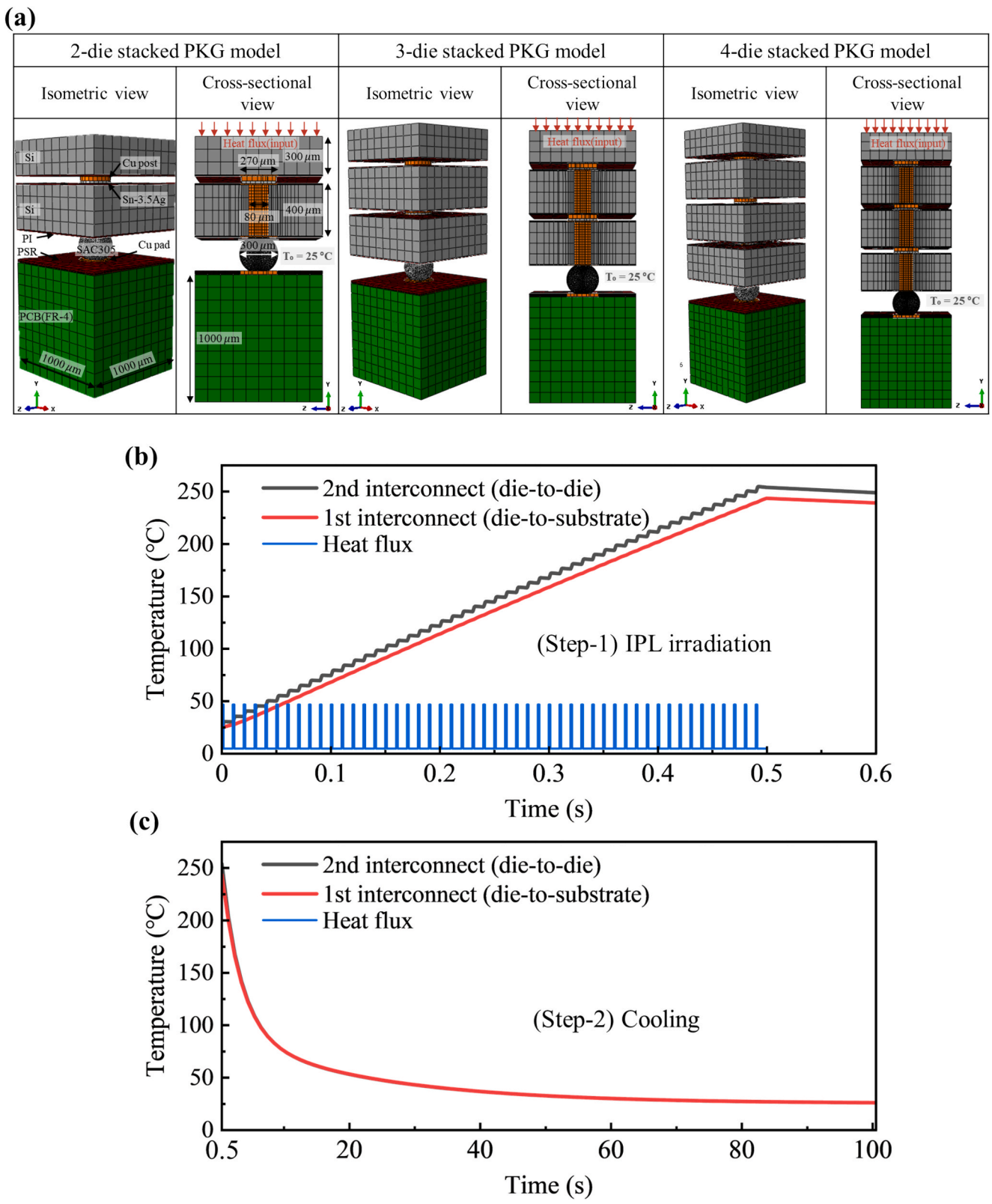

Fig. 3. (a) Finite element models for thermal transient simulation: isometric and cross-sectional views of 2-die, 3-die, and 4-die stacked packages with boundary conditions and material assignments. Representative simulated temperature profiles of the 2-die model (50 pulses) during (b) IPL irradiation (Step-1) and (c) natural cooling (Step-2) at the 1st and 2nd interconnection layers.

μm thick), Cu pad on PCB (Cu; 30 μm thick), and PCB substrate (FR-4; 1000 μm thick). All interfaces between the modeled components were treated as perfectly bonded using a tie constraint, since the solder joints form metallurgical bonds rather than mechanical contacts, as confirmed by the continuous interfacial IMC layers observed at every interconnection layer. The thermal properties listed in Table 2 were treated as temperature-independent, and phase change of the solder was not incorporated in the model.

The transient heat transfer analysis was performed in two sequential steps: Step-1 (IPL irradiation) with fine time increments (0.1 ms) to capture the rapid pulse on/off cycles, and Step-2 (natural cooling) with larger time increments (1 s), as the temperature changes gradually during the cooling phase. The transient heat transfer in both steps was governed by the following equation:

$$\rho c_p \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) + q \quad (1)$$

where ρ is the density, c_p is the specific heat capacity, T is the temperature, t is the time, k is the thermal conductivity, and q is the heat source term. The boundary conditions were as follows: (1) IPL heat flux of 4665 mJ/mm^2·s was applied on the top silicon surface during pulse on-time [18], calculated from the measured irradiation energy density (9330 mJ/mm^2·s) with an assumed silicon absorptivity of 50%. The IPL emission spectrum lies entirely within the absorption band of silicon, whose band gap of approximately 1.12 eV corresponds to a wavelength of about 1100 nm [22]. Since transmission through a 300–400 μ m die is negligible across this spectral range [23], the effective absorptivity is governed by surface reflection; weighting the wavelength-dependent absorptivity by the xenon lamp emission spectrum gives approximately 57% [24,25]. A conservative value of 50% was adopted to account for additional optical losses not captured in this idealized calculation, and this assumption was validated by the agreement between the simulated and measured temperature profiles in our previous study [18]; (2) natural convection with a heat transfer coefficient of 10 W/m^2·K was applied to all surfaces exposed to air; and (3) radiation with emissivity of 0.7, corresponding to a polished silicon surface was applied to the top silicon surface [26]. The ambient temperature was set to 298 K. Fig. 3(b-c) show representative simulated temperature profiles for the 2-die model (50 pulses) during the IPL irradiation (Step-1) and natural cooling (Step-2) phases, respectively.

2.4. Characterization

The microstructure and composition of solder joints were investigated using field-emission scanning electron microscopy (FE-SEM) with energy-dispersive spectroscopy (EDS) (Quattro E-SEM, Thermo Fisher Scientific Inc.). Cross-sectional samples were prepared by standard metallographic techniques including cold mounting, grinding, and polishing. The IMC thickness was quantitatively measured using an automated image processing method based on Otsu thresholding [33] applied to backscattered electron (BSE) cross-sectional images, as detailed in the Supporting Information (Fig. S3). For each interconnection layer, one solder joint was sampled from each of the six rows of the 6 × 6 bump arrays, and a BSE image at 10,000 × magnification was acquired from each joint. The IMC thickness was determined as the segmented IMC area divided by the width of the field of view, giving an area-averaged thickness over the imaged interface. Since the field of view at this magnification spans multiple scallop peaks and valleys, the local morphological variation is integrated within each measurement. Every segmentation result was overlaid on the original image and inspected visually, and the segmentation was corrected manually where the automated threshold did not delineate the IMC boundary correctly. The standard deviations reported in this work therefore represent the variation among the six sampled joints in each layer.

Table 2
Thermal properties of materials used in the finite element simulation model.

Material	Density (kg/m^3)	Thermal conductivity (W/m•K)	Heat capacity (J/kg·K)
Si[27]	2230	163	703
Cu[27]	8700	400	385
PSR[28]	1570	0.23	1140
PI[29]	1430	0.2	1084
Sn-3.5Ag[30,31]	7370	50[a]	220
SAC305[18]	7380	58	230
PCB(FR-4)[32]	1800	0.29	1150

[a] AMETEK Electronic Components and Packaging, 96.5 Tin-3.5 Silver Data Sheet, Coining Inc., Montvale, NJ, USA.

2.5. Thermal Cycling Reliability Test

Thermal cycling (TC) reliability tests were performed using a thermal cycling chamber to evaluate the long-term thermomechanical reliability of the multi-die stacked packages. The temperature was cycled between 0 °C and 125 °C, with a ramp time of 5 min, dwell time of 5 min at both the upper and lower temperature extremes, and a total cycle duration of approximately 20 min. The measured temperature profile using thermocouples is provided in the Supporting Information (Fig. S4). The electrical resistance of the outer daisy chain line was continuously monitored in real-time during thermal cycling using a LabVIEW-based data acquisition system (NI-9219). The outer line was selected for monitoring because it has the largest distance from the neutral point and therefore experiences the highest CTE-mismatch strain, so that failure occurs there first. Based on the failure criteria outlined in IPC-9701, failure was defined as a 20% increase in resistance sustained for five consecutive measurements [34,35]. The TC tests were conducted for all stack configurations (2-, 3-, and 4-die) bonded by both IPL and mass reflow processes with five specimens tested for each condition.

3. Results and discussion

3.1. FEM Thermal Simulation and IPL Bonding Process Optimization

Fig. 4 presents the simulated peak temperatures at each interconnection layer as a function of pulse number for the 2-die (Fig. 4(a)), 3-die (Fig. 4(b)), and 4-die (Fig. 4(c)) stacked packages. In all configurations, the peak temperature increases linearly with pulse number at each interconnection layer. This is attributed to the proportional increase in cumulative energy input with the number of IPL pulses. In addition, a consistent temperature gradient was observed across the stack. The uppermost interconnection layer closest to the IPL irradiation source exhibits the highest peak temperature, while progressively lower layers show decreasing peak temperatures.

This gradient is a direct consequence of the photothermal heating mechanism demonstrated in our previous study [18]. The top silicon die absorbs the irradiated IPL energy and converts it into heat, which is subsequently conducted downward through the stacked dies. In the multi-die configuration, this top-down heat conduction path results in a gradual decrease in thermal energy reaching the lower interconnection layers. Consequently, at the same pulse number, packages with more stacked dies exhibit consistently lower peak temperatures at all interconnection layers. For example, at 50 pulses, the topmost interconnection layer reaches approximately 254 °C in the 2-die stack (2nd interconnect; Fig. 4(a)), whereas it reaches only approximately 192 °C in the 3-die stack (3rd interconnect; Fig. 4(b)). This is because additional die layers increase the total thermal mass of the structure.

Due to the inherent temperature gradient of the IPL process, the optimal pulse number for each configuration must be determined as the minimum number of pulses at which the bottommost interconnection layer exceeds the melting temperature of SAC305 (T_m = 217 °C) [36]. As

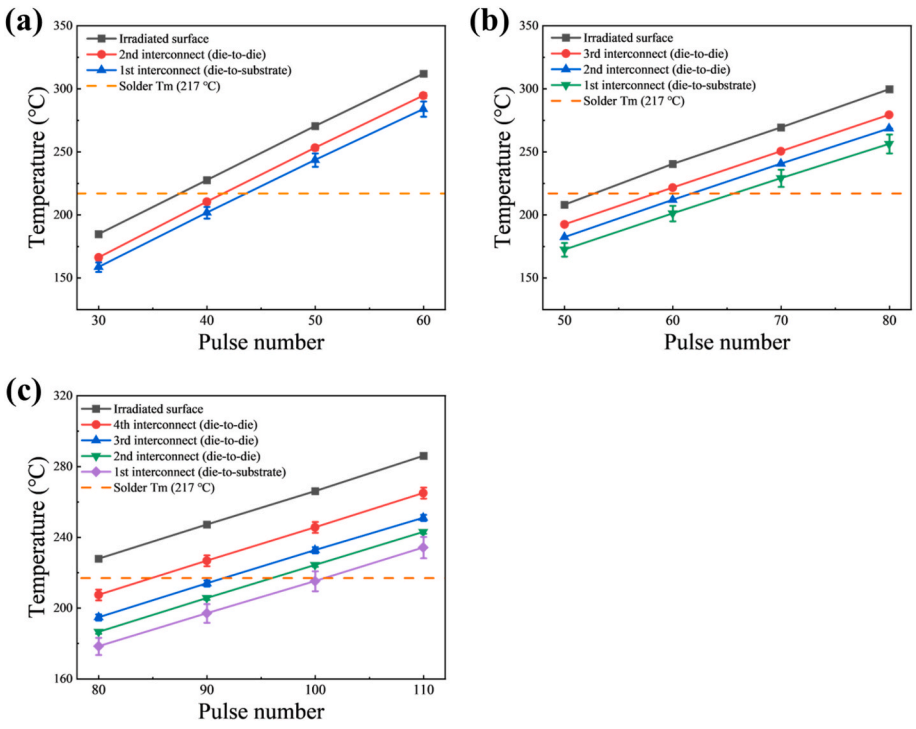

Fig. 4. Simulated peak temperatures at each interconnection layer as a function of pulse number for (a) 2-die, (b) 3-die, and (c) 4-die stacked packages. The dashed line indicates the SAC305 melting temperature (217 °C). Error bars represent the standard deviation of peak temperatures across multiple nodes at each interconnection layer.

shown in Fig. 4, at 50, 70, and 110 pulses, the bottommost (1st) interconnection layer reached approximately 244, 229, and 233 °C for

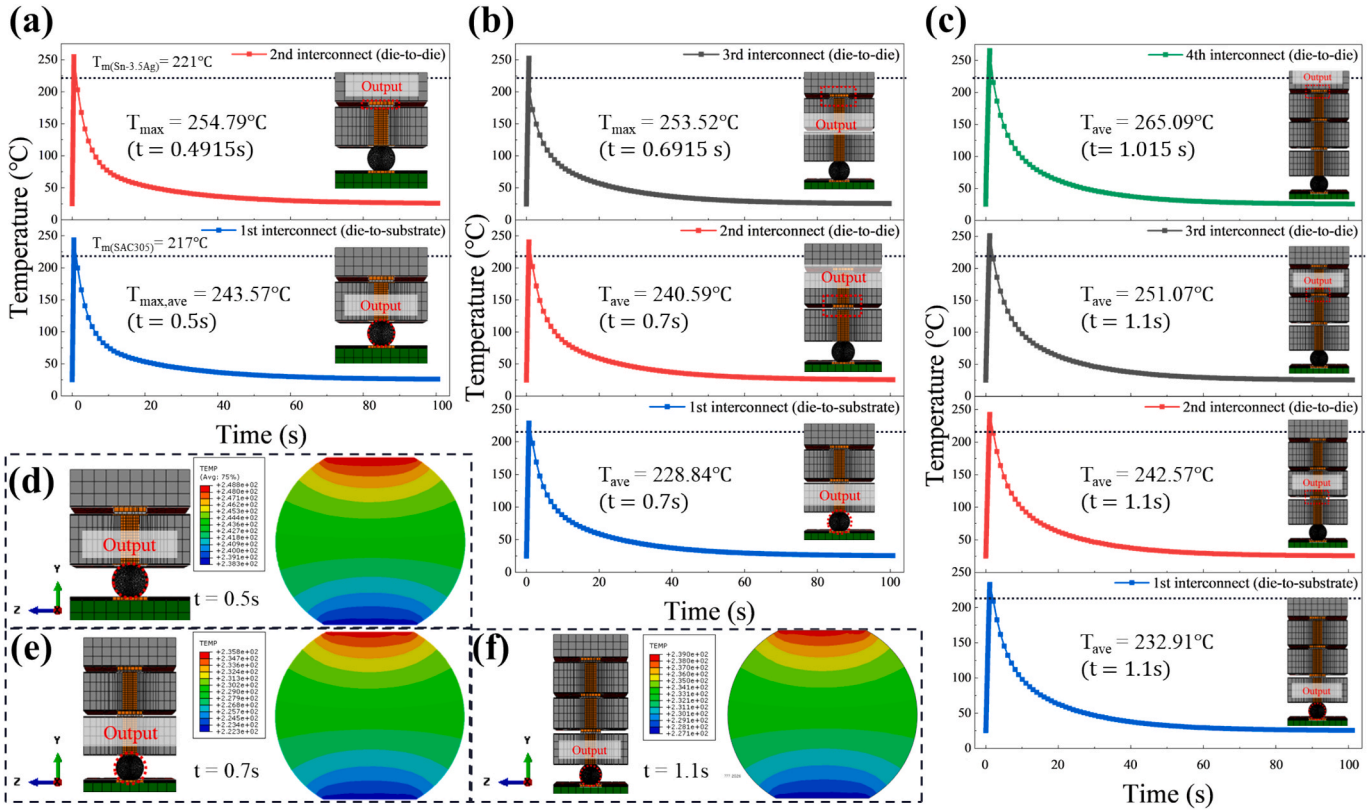

Fig. 5. Simulated temperature profiles at each interconnection layer under optimized IPL conditions: (a) 2-die with 50 pulses, (b) 3-die with 70 pulses, and (c) 4-die with 110 pulses. Temperature contour maps of the 1st interconnection (die-to-substrate) solder ball for (d) 2-die at t = 0.5 s, (e) 3-die at t = 0.7 s, and (f) 4-die at t = 1.1 s. The dashed lines indicate the melting temperatures of Sn-3.5Ag (221 °C) and SAC305 (217 °C).

the 2-die, 3-die, and 4-die stacks, respectively, all exceeding the solder melting point. Accordingly, the experimental conditions for each configuration were determined as 50, 70, and 110 pulses, as shown in Table 1. It should be noted that this melting criterion establishes the minimum pulse number required, and joint formation was subsequently verified experimentally through cross-sectional microstructural analysis (Section 3.2) and the electrical continuity of the daisy chain lines (Table S1), rather than being inferred from the thermal simulation alone.

Fig. 5 shows the simulated temperature profiles at each interconnection layer under the optimized IPL pulse number. For the 2-die stack with 50 pulses (Fig. 5(a)), the 2nd interconnection (die-to-die) reached a peak temperature of approximately 254.79 °C, while the 1st interconnection (die-to-substrate) reached approximately 243.57 °C. For the 3-die stack with 70 pulses (Fig. 5(b)), the peak temperatures ranged from approximately 253.52 °C (3rd interconnection) to 228.84 °C (1st interconnection). For the 4-die stack with 110 pulses (Fig. 5(c)), the peak temperatures ranged from approximately 265.09 °C (4th interconnection) to 232.91 °C (1st interconnection). Fig. 5(d–f) shows the temperature contour maps of the 1st interconnection solder ball at the maximum temperature point. All interconnection layers exceeded the respective solder melting temperatures (221 °C for Sn-3.5Ag [37] at die-to-die interfaces, 217 °C for SAC305 [36] at die-to-substrate interface), indicating that all interconnection layers can achieve successful solder melting and joint formation under those conditions.

Beyond peak temperature, the TAL and cooling rate at each layer are also critical for understanding IMC growth behavior. Table 3 summarizes the peak temperature, TAL, and cooling rate at each interconnection layer. As shown in Table 3, the upper interconnection layers not only exhibit higher peak temperatures as discussed above, but also significantly longer TAL. For example, in the 4-die stack, the peak temperature difference between the 4th and 1st interconnection layers is approximately 32 °C, while the TAL difference reaches approximately 540 ms. This TAL gradient occurs because the upper layers accumulate heat more rapidly as they are closer to the IPL source. As a result, they exceed the solder melting temperature earlier and remain above it for a longer duration. Since IMC growth is primarily governed by liquid/solid interfacial reaction time [38–40], thicker IMC formation is expected at the upper interconnection layers where TAL is longer.

The cooling rates also decrease with increasing stacked dies, from approximately 8.0 °C/s for the 2-die stack to 7.0 °C/s for the 3-die stack and 6.7 °C/s for the 4-die stack (Table 3). This is because the additional die layers increase the total thermal mass of the structure, slowing overall heat dissipation. Since higher cooling rates are known to suppress IMC growth by limiting the time available for solid-state diffusion [41], this reduction in cooling rate further contributes to IMC formation in packages with more stacked dies. Consequently, the upper interconnection layers in packages with more stacked dies experience the combined effect of higher peak temperatures, longer TAL, and slower cooling rates, all of which promote IMC growth [38–41]. Therefore, the uppermost layer of the 4-die stack is expected to exhibit the thickest IMC formation after IPL irradiation.

Table 3
Simulated peak temperature, TAL, and cooling rate at each interconnect layer for IPL-bonded multi-die stacked packages.

PKG (pulse number)	Layer	Peak Temperature (°C)	TAL (ms)	Cooling rate[a] (°C/s)
2-die (#50)	2nd interconnection (die-to-die)	254.79	727	8.0
	1st interconnection (die-to-substrate)	243.57	669	7.8
3-die (#70)	3rd interconnection	253.52	697	7.0
	2nd interconnection	240.59	541	7.0
	1st interconnection	228.84	384	6.7
4-die (#110)	4th interconnection	265.09	1097	6.7
	3rd interconnection	251.07	981	6.7
	2nd interconnection	242.57	850	6.7
	1st interconnection	232.91	557	6.6

[a] Average cooling rate from T_m to 50 °C.

3.2. Microstructural Analysis of IPL-Bonded Multi-die Stacked Packages

Prior to microstructural analysis, the as-bonded electrical continuity of all specimens was verified by measuring the resistance of the three daisy chain lines (Table S1). Since each line connects all interconnection layers in series and the three lines together cover the entire die area, the continuity of all lines in all specimens confirms that metallurgical joints were formed at every interconnection in every layer. To experimentally verify the thermal predictions from the FEM simulation and the anticipated IMC thickness gradient across the interconnection layers, cross-sectional SEM analysis was performed on the IPL-bonded multi-die stacked packages. Fig. 6 shows the cross-sectional SEM images of the 4-die stacked package bonded by the IPL process (110 pulses). Continuous solder joints were successfully formed at all interconnection layers, including the 4th (die-to-die), 3rd (die-to-die), 2nd (die-to-die), and 1st (die-to-substrate) interconnections (Fig. 6(b–e)). No cracks or interfacial defects were observed at this magnification. Similarly, robust solder joints were confirmed at all interconnection layers in the 2-die and 3-die stacked packages (see Supporting Information, Fig. S5).

To further investigate the interfacial reactions at each interconnection layer, EDS elemental mappings (Cu, Sn, Ag, Ni) were performed, as shown in Fig. 7. At the die-to-die interfaces (Fig. 7(a–c)), Cu and Sn signals were concentrated at the interface between the Cu pad and the Sn-3.5Ag solder (Fig. 7(a-1–c-1, a-2–c-2)), indicating the formation of a Cu–Sn intermetallic compound. Ag was distributed as fine precipitates within the solder matrix (Fig. 7(a-3, b-3, c-3)). Ni signal was also detected at the IMC layer (Fig. 7(a-4, b-4, c-4)), originating from the Ni barrier layer in the UBM structure. At the die-to-substrate interface (Fig. 7(d)), the IMC layer formed between the SAC305 solder ball and the Cu pad of the OSP-finished PCB substrate, with Cu and Sn signals concentrated at the interface (Fig. 7(d-1, d-2)). The apparent Ni signal near the Cu pad region in Fig. 7(d-4) does not indicate the actual presence of Ni. This artifact arises from the spectral overlap between Cu-Lα (0.930 keV) and Ni-Lα (0.851 keV) characteristic X-ray energies.

Since the upper IMCs of all interconnects were initially formed during the specimen fabrication process (solder ball attachment on wafer), the following analysis focuses on the lower interface IMC of each interconnect, which is formed during the IPL bonding process. Fig. 8 shows the EDS point analysis results comparing the IMC composition at the die-to-die interface (Point 1) and the die-to-substrate interface (Point 2). At the die-to-die interface, the atomic percentages of Cu, Sn, and Ni were approximately 57%, 41%, and 2%, respectively (Fig. 8(b)), consistent with the $(Cu,Ni)_6Sn_5$ stoichiometry. The Ni originates from the UBM barrier layer and partially substitutes for Cu in the IMC lattice. At the die-to-substrate interface, the composition was approximately Cu 59% and Sn 40%, with negligible Ni content, consistent with the Cu_6Sn_5 stoichiometry, as expected for the OSP-finished PCB substrate without a Ni barrier layer. The Ag signal detected at Point 1 (0.4%) likely originates from nearby Ag_3Sn precipitates captured within the EDS interaction volume. These phase assignments are inferred from the measured elemental compositions and were not independently confirmed by structural characterization.

3.3. IMC Thickness Gradient and Correlation with Temperature Distribution

Fig. 9 shows the measured IMC thickness and FEM-predicted peak

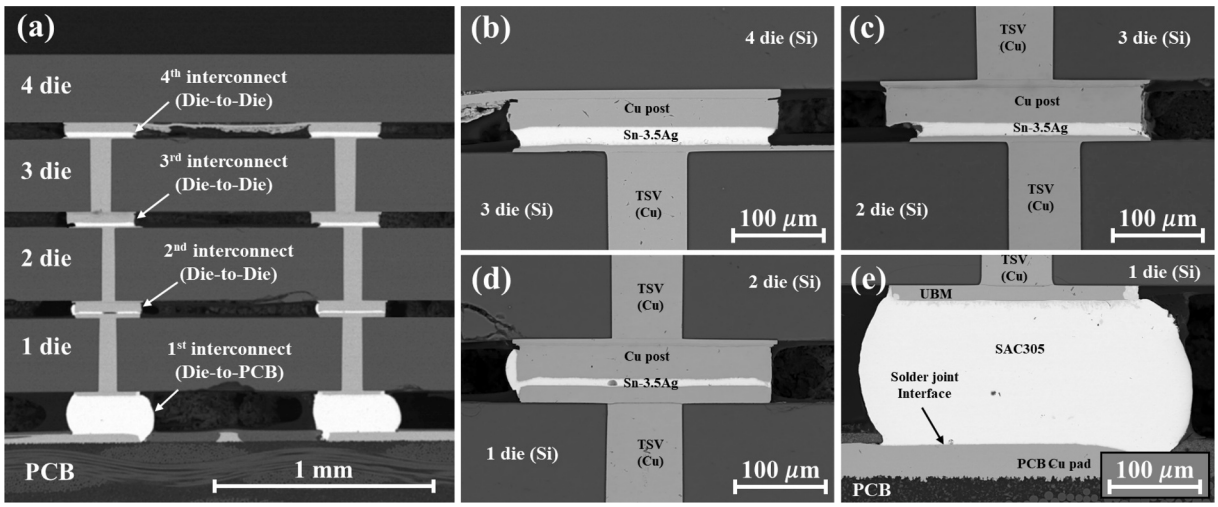

Fig. 6. Cross-sectional SEM images of the 4-die stacked package bonded by the IPL process: (a) overall cross-section showing all interconnection layers and enlarged views of (b) 4th interconnection (die-to-die), (c) 3rd interconnection (die-to-die), (d) 2nd interconnection (die-to-die), and (e) 1st interconnection (die-to-substrate).

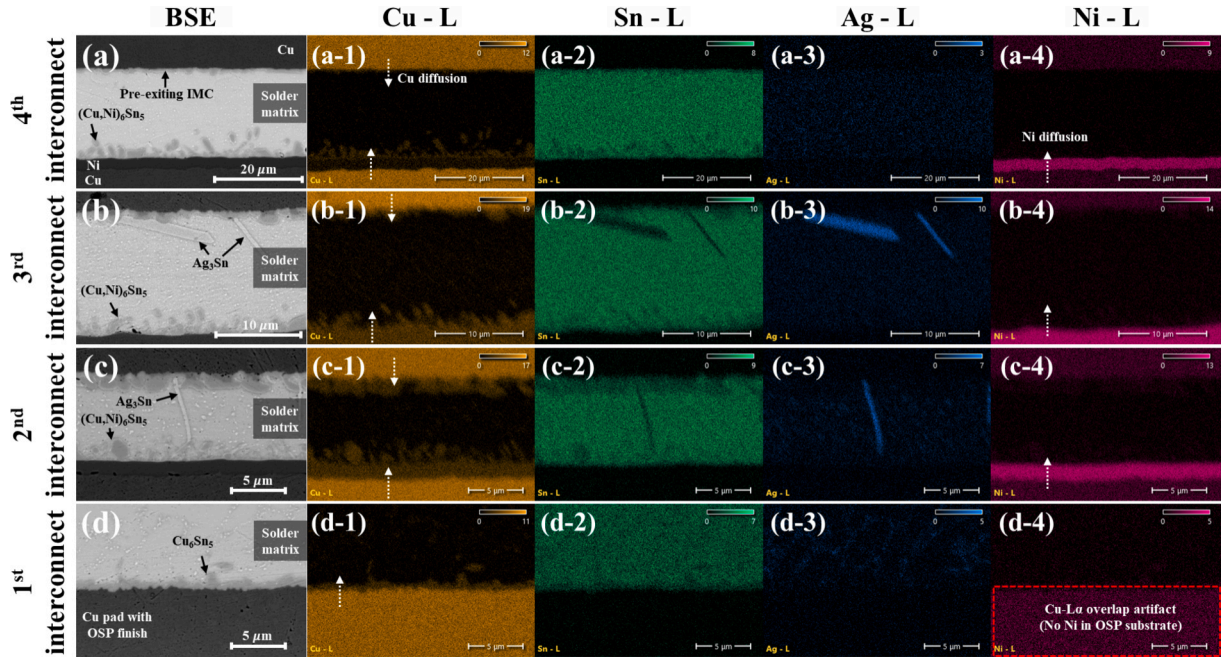

Fig. 7. Cross-sectional BSE-SEM images and EDS elemental mappings (Cu, Sn, Ag, Ni) of solder joint interfaces in the 4-die stacked package bonded by the IPL process: (a) 4th interconnection (die-to-die), (b) 3rd interconnection (die-to-die), (c) 2nd interconnection (die-to-die), and (d) 1st interconnection (die-to-substrate). Each row shows the SEM image followed by EDS mappings of Cu-L (a-1 to d-1), Sn-L (a-2 to d-2), Ag-L (a-3 to d-3), and Ni-L (a-4 to d-4).

temperature at each interconnection layer for the 2-die (Fig. 9a), 3-die (Fig. 9b), and 4-die (Fig. 9c) stacked packages bonded by the IPL process. The IMC thickness was quantitatively measured using the digital image analysis method described in Section 2.4 (see Supporting Information, Fig. S3 for the detailed procedure). Across all configurations, the IMC thickness consistently decreases from the uppermost to the lowermost interconnection layer, showing a clear correlation with the FEM-predicted peak temperature. For example, in the 4-die stack, the IMC thickness ranges from approximately 2.01 ± 1.00 μm at the 4th interconnection (peak temperature: 265.09 °C) to 0.78 ± 0.23 μm at the 1st interconnection (232.91 °C). Similar trends were observed in the 2-die and 3-die stacks (Fig. 9(a, b)). These results confirm that the layer-by-layer TAL gradient and peak temperature are the main factors driving the variation in IMC thickness, as predicted in the FEM thermal analysis in Section 3.1.

In addition to the mean thickness gradient, the variation in IMC thickness also showed a systematic trend. Notably, the standard deviation of the IMC thickness was larger at the upper interconnection layers compared to the lower layers across all configurations. This trend can be directly observed in the SEM images of Fig. 7. The 4th interconnection (Fig. 7(a)) exhibits a pronounced scallop-type IMC morphology with significant local thickness variation, whereas the 1st interconnection (Fig. 7(d)) shows a thinner and more planar IMC layer. This morphological transition from scallop-type to planar IMC is attributed to the higher peak temperatures and longer TAL at the upper layers. It has been reported that higher temperatures and longer TAL promote greater Cu dissolution and subsequent scallop growth and coarsening at the Cu–Sn interface [42,43]. Therefore, the characteristic scallop structure with inherently larger thickness variation at the upper layers is attributed to the thermal gradient inherent to the IPL bonding process.

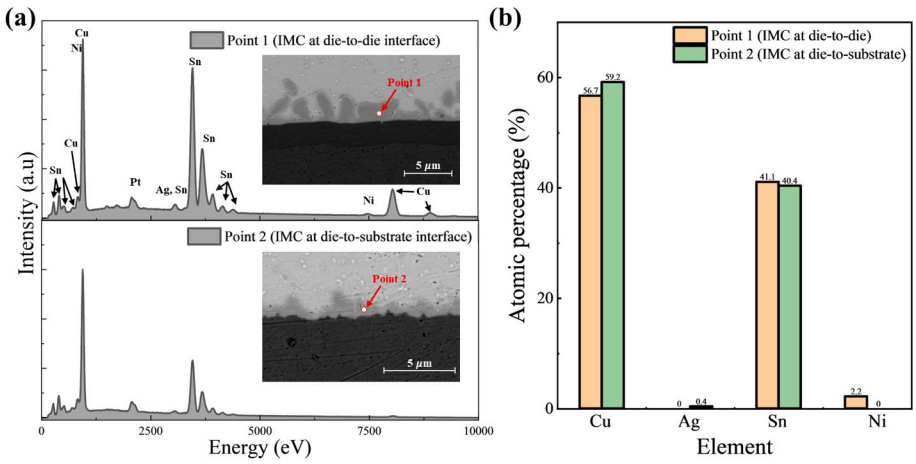

Fig. 8. (a) EDS point analysis spectra of IMC layers at die-to-die interface (Point 1) and die-to-substrate interface (Point 2), with corresponding BSE-SEM images showing measurement locations. (b) Quantitative atomic composition comparison of Cu, Ag, Sn, and Ni at the two IMC interfaces.

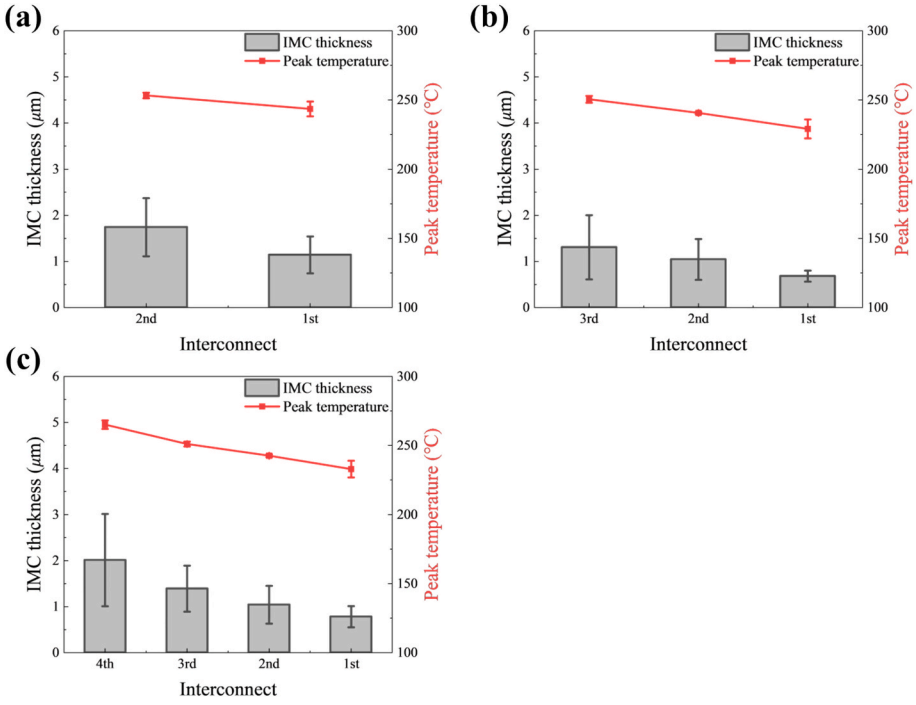

Fig. 9. IMC thickness and simulated peak temperature at each interconnection layer for (a) 2-die, (b) 3-die, and (c) 4-die stacked packages bonded by the IPL process. The bar charts represent the measured IMC thickness (left axis), and the red line indicates the simulated peak temperature (right axis). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

3.4. Comparison with Mass Reflow Process

Table 4 compares the process conditions and thermal characteristics between the multi-die IPL process, and conventional mass reflow process. The key differences are the dramatically shorter TAL (384–1097 ms vs. ~60,000 ms) and faster cooling rates (6.6–8.0 vs. ~3 °C/s) of the IPL process. Additionally, unlike the uniform temperature of mass reflow, the IPL process produces an inherent temperature gradient (ΔT = 11.2–32.2 °C). Despite these fundamental differences in thermal history, the IPL process achieved successful solder joint formation at all interconnection layers, as confirmed by the FEM simulation (Section 3.1) and cross-sectional SEM analysis (Section 3.2).

Fig. 10(a) shows the cross-sectional SEM images comparing the IMC morphology at each interconnection layer between the mass reflow and IPL bonding processes for the 4-die stacked package. In the mass reflow samples, thick and irregularly shaped scallop-type IMC layers were observed at all interconnection layers, with relatively uniform thickness across different die levels. This uniformity arises because the convection-based heating mechanism exposes all interconnection layers to the same peak temperature (250 °C) for the same duration regardless of the layer position. In addition, micro voids were frequently observed within the thick IMC layers at the 4th, 3rd, and 2nd interconnection layers, and a crack was also identified at the 2nd interconnection layer (see Fig. 10(a)). Specifically, these micro voids are located at and immediately above the interfacial IMC layer rather than being randomly distributed within the solder matrix, and are attributed to the Kirkendall effect, where the asymmetric diffusion rates of Cu and Sn during prolonged high-temperature exposure generate vacancy accumulation at the Cu side of the interface [44,45]. The crack formation, on the other hand, is associated with the brittle nature of the thick IMC layer, which

Table 4
Comparison of process conditions and thermal characteristics between the IPL bonding process, and conventional mass reflow process.

	2-die	3-die	4-die	Reflow
Pulses (Counts)	50	70	110	—
IPL irradiation time (s)	0.5	0.7	1.1	300[a]
ΔT[b] (°C)	11.2	21.4	32.2	—
TAL range[c] (ms)	669–727	384–697	557–1097	60,000
Cooling rate[d] (°C/s)	7.8–8.0	6.7–7.0	6.6–6.7	3

[a] Total reflow profile time including preheat, soak, reflow, and cooling stages.
[b] ΔT represents the difference in peak temperature between the topmost and bottommost interconnect layers.
[c] Values represent the range across interconnect layers; T_m refers to 221 °C for Sn-3.5Ag and 217 °C for SAC305.
[d] Average cooling rate from T_m to 50 °C.

fractures under thermal stress induced by CTE mismatch during the bonding process [46,47]. Such defects may serve as potential failure initiation sites under thermomechanical loading [47]. In contrast, the IPL-bonded samples exhibited noticeably thinner IMC layers at all interconnection layers. While occasional micro voids were observed at the upper interconnection layers where the IMC was relatively thicker, their frequency and size were reduced compared to the reflow samples, and no cracks were identified. Their occurrence at the upper layers is attributed to the same Kirkendall mechanism described above, as the higher peak temperature and longer TAL at these layers promote greater Cu–Sn interdiffusion. Similar trends were observed in the 2-die and 3-die stacked packages, where the IPL-bonded samples consistently exhibited thinner IMC layers with fewer defects compared to the mass reflow samples (see Supporting Information, Fig. S5).

Fig. 10(b) provides the quantitative comparison of IMC thickness between mass reflow and IPL bonding at each interconnection layer for all three stack configurations. In the mass reflow process, the IMC thickness ranged from approximately 2.5 to 3.5 μm with relatively uniform distribution across different interconnection layers. In the IPL process, the IMC thickness ranged from approximately 0.7 to 2.0 μ m, with the gradient correlating to the FEM-predicted temperature distribution. Overall, the IPL process achieved IMC thickness reductions of approximately 29–78% compared to the mass reflow process, depending on the interconnection layer position. This significant reduction is a direct result of the dramatically shorter TAL (384–1097 ms vs. ~60,000 ms) and faster cooling rates (6.6–8.0 vs. ~3 °C/s) of the IPL process, which effectively limit the time available for interfacial diffusion reactions. Notably, the largest reduction was observed at the lowermost interconnection layers. Because the mass reflow process produces nearly uniform IMC thickness across all layers regardless of position, whereas the IPL process generates the thinnest IMC at the lower layers due to the shortest TAL and lowest peak temperature, the difference between the two processes is maximized at the lowermost interconnection layers.

3.5. Thermal Cycling Reliability of Multi-die Stacked Packages

Fig. 11 shows the representative in-situ resistance monitoring results for both the IPL-bonded and the mass reflow packages during the thermal cycling test (0–125 °C, 5-min dwell; see Section 2.5 for details). The failure criterion was defined as a 20% resistance increase sustained for five or more consecutive cycles, in accordance with IPC-9701A [34,35]. Note that in all cases, the thermal fatigue failure occurred at the corner of the package, where the distance from neutral point is the greatest. Two distinct resistance degradation patterns were identified across the tested specimens. The first is a gradual resistance increase, which is characteristic of progressive crack propagation within the solder joint. The second is repeated resistance spikes followed by recovery to near-baseline levels. This pattern is caused by interface delamination, where the delaminated surfaces intermittently re-contact during thermal cycling and temporarily restore electrical continuity.

The 2-die IPL package (Fig. 11(a)) exhibited the most robust reliability, sustaining 79 cycles before failure with a gradual increase in resistance. The 3-die and 4-die IPL packages (Fig. 11(c, e)) showed

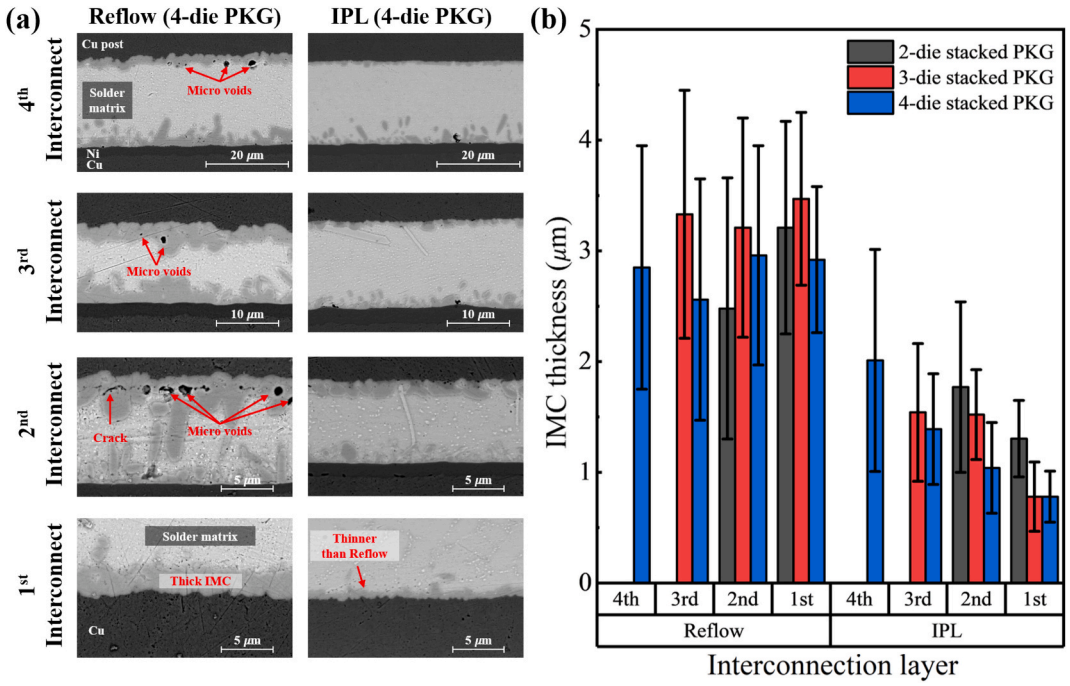

Fig. 10. (a) Cross-sectional SEM images comparing IMC morphology at each interconnection layer between mass reflow and IPL bonding for the 4-die stacked package. **(b)** Quantitative comparison of IMC thickness between mass reflow and IPL bonding at each interconnection layer for 2-die, 3-die, and 4-die stacked packages.

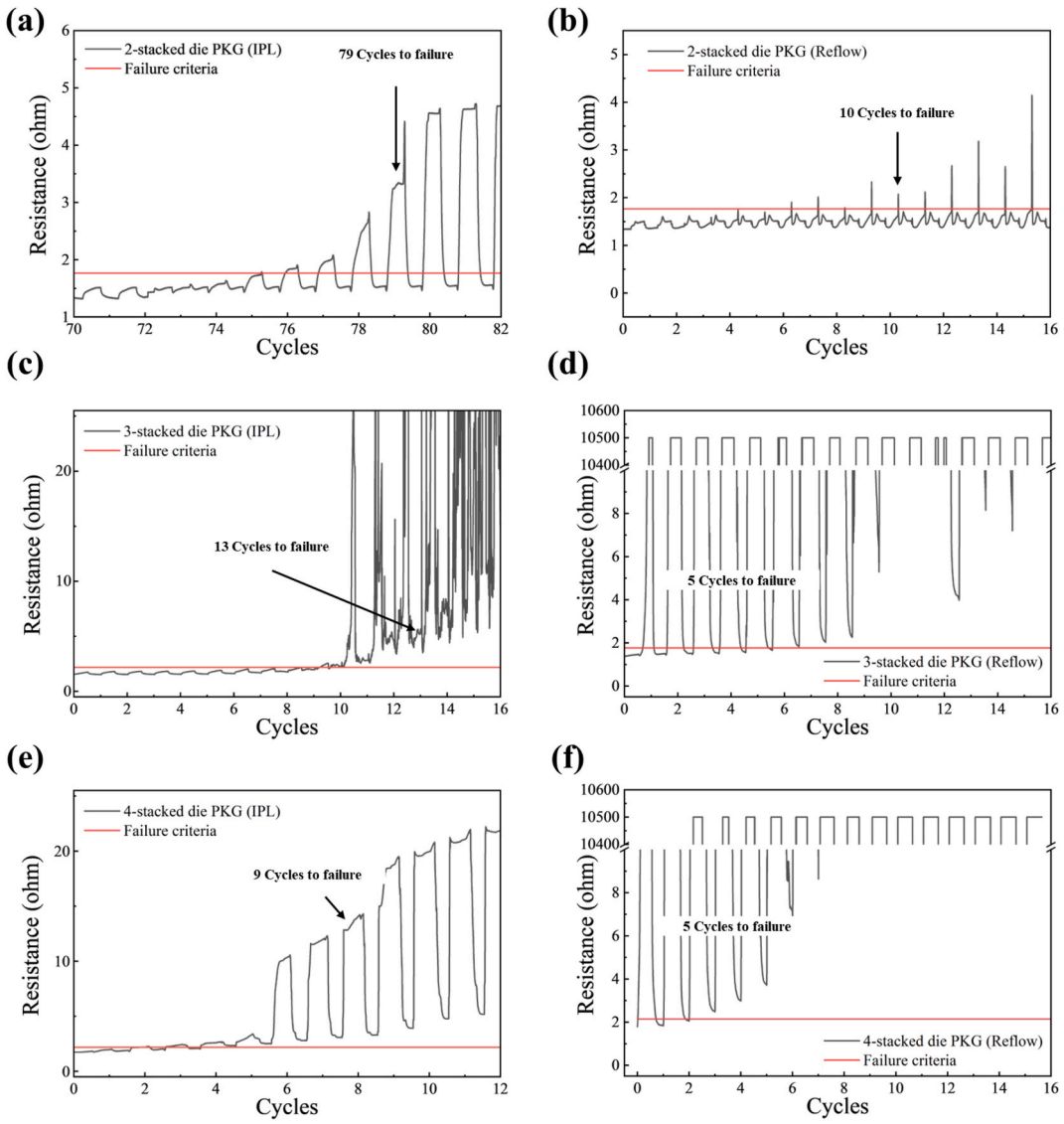

Fig. 11. Representative electrical resistance variations during thermal cycling reliability testing for multi-die stacked packages: (a) 2-die stacked package (IPL), (b) 2-die stacked package (Reflow), (c) 3-die stacked package (IPL), (d) 3-die stacked package (Reflow), (e) 4-die stacked package (IPL), and (f) 4-die stacked package (reflow).

failure at 13 and 9 cycles, respectively, with intermittent resistance spikes prior to failure. For the reflow packages, the reflow 2-die package (Fig. 11(b)) showed periodic resistance spikes in the initial cycles. This suggests that interfacial cracks grew progressively before eventually leading to delamination failure. On the other hand, the 3-die and 4-die configurations exhibited open-circuit behavior (>10 kΩ) from the earliest cycles (Fig. 11(d, f)), indicating that interface delamination occurred almost immediately upon thermal cycling. Furthermore, as the number of stacked dies increases, the greater total specimen thickness amplifies the cumulative thermomechanical strain induced by CTE mismatch, accelerating the interfacial degradation [12].

Fig. 12 compares the average cycles to failure between the mass reflow and IPL-bonded packages across all configurations, with the corresponding failure modes annotated. The IPL 2-die package exhibited the highest reliability among all conditions, sustaining approximately 71 cycles on average. In contrast, the remaining configurations showed significantly shorter fatigue life. The IPL 3-die and 4-die packages sustained approximately 17.6 and 12.4 cycles, while the corresponding reflow packages failed at approximately 15, 7.4, and 6.6 cycles for the 2-die, 3-die, and 4-die configurations, respectively.

To identify the failure mechanisms, post-TC cross-sectional SEM analysis was performed (Fig. 13). As shown in Fig. 12, the dominant failure mode for all conditions except the IPL 2-die package was TSV cracking and Cu pad delamination (Fig. 13(a)). The failure process can be understood as a sequential degradation mechanism involving two distinct stages: (1) interfacial degradation during the bonding process and (2) crack propagation during thermal cycling. During the bonding process, CTE mismatch between the constituent materials generates thermomechanical stress that can degrade interfacial adhesion at internal interfaces such as TSV/Si, Cu pad/substrate, and UBM/solder boundaries (Cu: ~17, Si: ~2.7, FR-4: ~17, Ni: ~13, and Solder: ~24.5 ppm/°C)[48–50]. Subsequently, during thermal cycling, repeated thermal loading drives crack initiation and propagation at these pre-weakened interfaces.

For all reflow packages, the prolonged high-temperature exposure (TAL ~60,000 ms) during the bonding process generates sustained thermomechanical stress from CTE mismatch, which degrades the interfacial adhesion at internal interfaces such as TSV/Si and Cu pad/substrate boundaries prior to thermal cycling. This degradation occurs independently of the stack height, which is why the 2-die reflow package

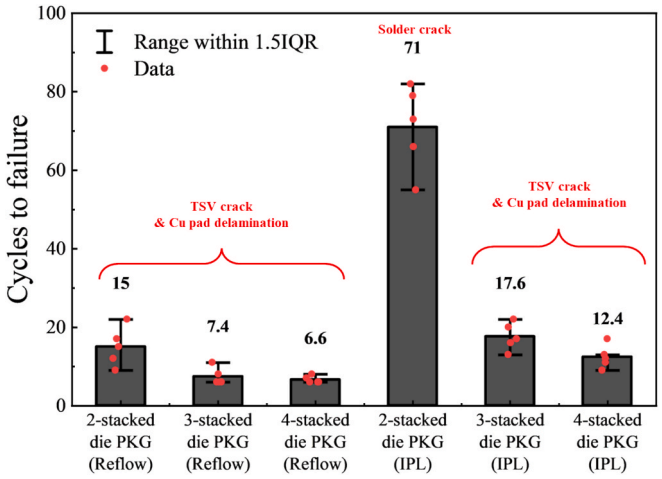

Fig. 12. Average cycles to failure for mass reflow and IPL-bonded multi-die stacked packages (n = 5 for each condition). Red dots indicate the individual measurements, and error bars represent the range within 1.5 IQR. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

also failed by TSV cracking despite having the same number of layers as the IPL 2-die package. For the IPL 3-die and 4-die packages, the ultrafast bonding process significantly reduces the thermal exposure, thereby mitigating the bonding-induced interfacial degradation at internal interfaces compared to the reflow process. However, in these higher-stack configurations, the increased total specimen thickness amplifies the thermomechanical strain generated during thermal cycling due to greater CTE mismatch across the thicker structure. This TC-induced strain becomes the dominant factor driving interfacial failure, which is sufficient to initiate failure at the internal interfaces despite the reduced thermal exposure.

On the other hand, the IPL 2-die package exhibited a distinctly different failure mode (Fig. 13(b)). The crack initiated near the IMC/solder interface and propagated along both the IMC layer and through the solder matrix, rather than along the internal interfaces such as TSV/Si or Cu pad/substrate boundaries. This transition indicates that the combination of minimal thermal exposure from the ultrafast IPL process and the relatively low thermomechanical strain in the 2-die configuration effectively preserved the interfacial integrity, making the solder itself the weakest link under cyclic loading. These results demonstrate that the IPL bonding process can significantly enhance TC reliability by preserving the integrity of internal interfaces through ultrafast thermal processing. In particular, the solder crack failure mode observed in the IPL 2-die package indicates that the interfaces were sufficiently strengthened for the solder itself to fail first, providing the most direct evidence of the interfacial preservation effect of the IPL process.

It should be also noted that the absolute cycles to failure reported here are governed primarily by the characteristics of the test vehicle rather than by the bonding process. The specimens were assembled without underfill, employ relatively thick silicon dies (300–400 μ m), and have a coarse 1.0 mm ball pitch. In industrial multi-die packages, molded underfill distributes the CTE-mismatch strain and is essential for achieving lifetimes of hundreds to thousands of cycles, whereas unfilled joints in this study transfer this strain directly to the interconnects. The absolute lifetimes reported here are therefore not comparable with the thermal cycling lifetimes reported for MR-MUF HBM packages. Consistent with this, failure in all conditions except the IPL 2-die package occurred by TSV cracking and Cu pad delamination, which are structural features of the test vehicle rather than the solder joints formed during bonding. The thermal cycling results presented here should therefore be interpreted as a comparative evaluation of the two bonding processes under identical and deliberately severe conditions, rather than as a qualification of absolute package reliability.

4. Conclusion

In this study, the intense pulsed light (IPL) flip-chip bonding process was extended from single-die to multi-die stacked package configurations (2-die, 3-die, and 4-die). A validated FEM thermal model revealed that the IPL process inherently produces a top-down temperature and TAL gradient across the stack. The optimal pulse numbers were determined as 50, 70, and 110 for the respective configurations, based on the criterion that the bottommost interconnection layer must exceed the solder melting temperature. Cross-sectional SEM and EDS analyses

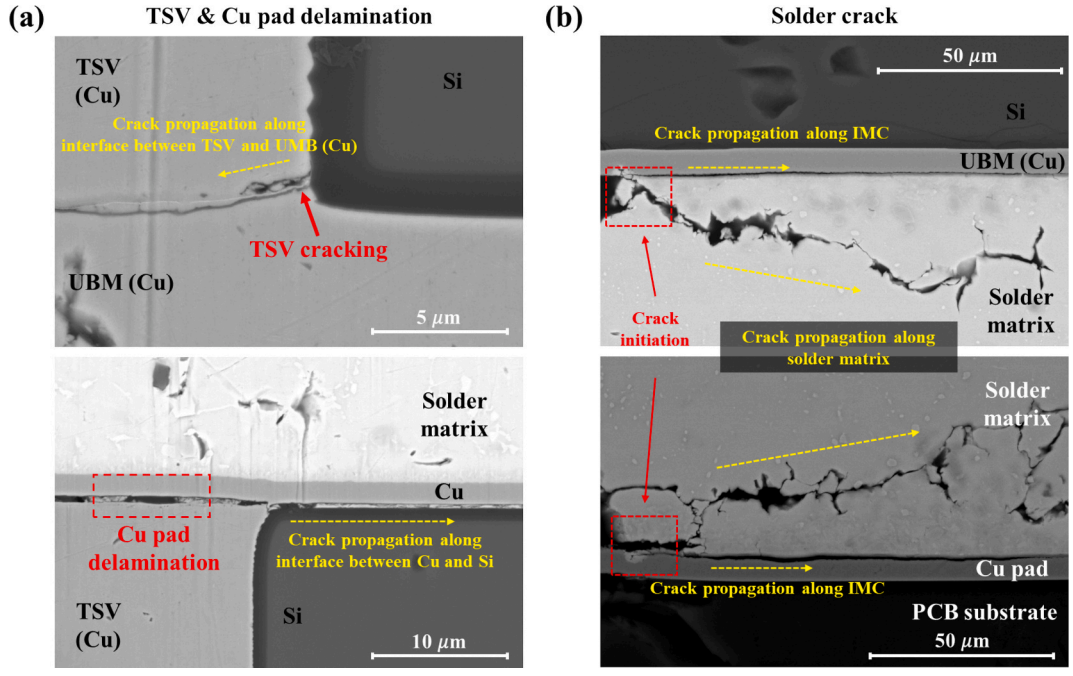

Fig. 13. Post-thermal cycling cross-sectional SEM images showing representative failure modes: **(a)** TSV cracking and Cu pad delamination and **(b)** solder crack.

confirmed successful solder joint formation at all interconnection layers, with $(Cu,Ni)_6Sn_5$ at the die-to-die interfaces and Cu_6Sn_5 at the die-to-substrate interfaces. The IMC thickness exhibited a clear layer-by-layer gradient (0.7–2.0 μm) consistent with the simulated thermal distribution. Compared to the mass reflow process, the IPL process achieved 29–78% thinner IMC layers, which is a direct result of the dramatically shorter TAL (384–1097 ms vs. ~60,000 ms) and faster cooling rates (6.6–8.0 vs. ~3 °C/s). Thermal cycling tests demonstrated that the IPL-bonded packages sustained 1.9–4.7 times more cycles to failure than the reflow counterparts. Post-TC failure analysis revealed that all conditions except the IPL 2-die package failed by TSV cracking and Cu pad delamination, driven by CTE-mismatch-induced interfacial degradation during the bonding process. Notably, the IPL 2-die package exhibited solder crack failure, where the crack propagated along the IMC layer and through the solder matrix rather than at the internal interfaces. This shift in failure mode provides direct evidence that the ultrafast IPL process preserves interfacial integrity by minimizing thermal exposure. These results demonstrate that the IPL bonding process offers a promising alternative to conventional mass reflow for multi-die stack assembly. We note that the present study was conducted on an unfilled test vehicle with relatively thick silicon dies (300–400 μ m) and a coarse ball pitch, and that reliability was assessed by thermal cycling alone. Establishing suitability for production therefore requires further verification under production-relevant conditions, including moisture sensitivity level (MSL), high-temperature storage (HTS), and drop impact testing, as well as evaluation with production-level die thicknesses (e.g., 40 μ m for HBM applications) and with underfill integration. Quantitative characterization of joint quality by X-ray CT and die-shear testing, assessment of package warpage under thin-die conditions, and thermo-mechanical analysis of the interfacial stress distribution are also identified as necessary next steps.

CRediT authorship contribution statement

Young-Min Ju: Writing – original draft, Visualization, Validation, Software, Methodology, Investigation, Data curation. **Hyeong-Bin Park:** Software, Investigation, Data curation. **Yun-Joong Kim:** Investigation, Data curation. **Hak-Sung Kim:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.matdes.2026.117151.

Data availability

Data will be made available on request.

References

[1] C.E. Leiserson, N.C. Thompson, J.S. Emer, B.C. Kuszmaul, B.W. Lampson, D. Sanchez, T.B. Schardl, There's plenty of room at the Top: What will drive computer performance after Moore's law? Science 368 (6495) (2020) eaam9744.
[2] K. Sakuma, P.S. Andry, C.K. Tsang, S.L. Wright, B. Dang, C.S. Patel, B.C. Webb, J. Maria, E.J. Sprogis, S.K. Kang, 3D chip-stacking technology with through-silicon vias and low-volume lead-free interconnections, IBM Journal of Research and Development 52 (6) (2008) 611–622.
[3] S. Borkar, 3D integration for energy efficient system design, Proceedings of the 48th Design Automation Conference, 2011, pp. 214-219.
[4] Y. Cheng, X. Guo, V.F. Pavlidis, Emerging monolithic 3D integration: Opportunities and challenges from the computer system perspective, Integration 85 (2022) 97–107.
[5] H. Jun, S. Nam, H. Jin, J.-C. Lee, Y.J. Park, J.J. Lee, High-bandwidth memory (HBM) test challenges and solutions, IEEE Design & Test 34 (1) (2016) 16–25.
[6] C.Y. Lee, C.H. Won, S. Jung, E.S. Jung, T.M. Choi, H.R. Lee, J. Yoo, S. Yoon, S. G. Pyo, 3D integrated process and hybrid bonding of high bandwidth memory (HBM), Electronic Materials Letters 21 (3) (2025) 395–419.
[7] S. Ahn, H. Kim, D.W. Kim, D. Hiner, K. Kim, T. Hwang, M. Lee, D. Kang, J. Yoon, Wafer level multi-chip gang bonding using TCNCF, 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), IEEE, 2016, pp. 122-127.
[8] C. Gerets, J. Derakhshandeh, P. Bex, M. Lofrano, V. Cherman, T. Cochet, K.J. Rebibis, G. Beyer, A. Miller, E. Beyne, TCB optimization for stacking large thinned dies with 40 and 20 μm pitch microbumps, 2018 7th Electronic System-Integration Technology Conference (ESTC), IEEE, 2018, pp. 1-6.
[9] T. Wang, P. Bex, G. Capuz, F. Duval, F. Inoue, C. Gerets, J. Bertheau, K.J. Rebibis, A. Miller, G. Beyer, 3D IC assembly using thermal compression bonding and wafer-level underfill—Strategies for quality improvement and throughput enhancement, 2016 IEEE 18th Electronics Packaging Technology Conference (EPTC), IEEE, 2016, pp. 791-796.
[10] S. Gokhale, K. Srinivasan, S. Zhong, A. Tripathi, High Precision Large Reticle Thermo-Compression Bonding for Advanced Packaging for AI Era, 2025 IEEE 75th Electronic Components and Technology Conference (ECTC), IEEE, 2025, pp. 1832-1836.
[11] K. Kim, M.-j. Park, Present and future, challenges of high bandwith memory (HBM), 2024 IEEE International Memory Workshop (IMW), IEEE, 2024, pp. 1-4.
[12] K.-N. Tu, Reliability challenges in 3D IC packaging technology, Microelectronics Reliability 51 (3) (2011) 517–523.
[13] Z. Zhang, J. Kim, D. Won, Statistical-based simulation and reflow profile optimization for improving self-alignment performance– an experimental study, Soldering & Surface Mount Technology 37 (4) (2025) 258–268.
[14] Y. Wang, I.M. De Rosa, K.-N. Tu, Size effect on ductile-to-brittle transition in Cu-solder-Cu micro-joints, 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), IEEE, 2015, pp. 632-639.
[15] Q. Zhang, Z. Zhang, In-situ observations on fracture behaviors of Cu–Sn IMC layers induced by deformation of Cu substrates, Materials Science and Engineering: A 530 (2011) 452–461.
[16] M. Alam, H. Lu, C. Bailey, Y.C. Chan, Fracture mechanics analysis of solder joint intermetallic compounds in shear test, Computational Materials Science 45 (2) (2009) 576–583.
[17] W. Alves Braganca, Y.S. Eom, K.S. Jang, S.H. Moon, H.C. Bae, K.S. Choi, Collective laser-assisted bonding process for 3D TSV integration with NCP, Etri Journal 41 (3) (2019) 396–407.
[18] Y.-M. Ju, S.-U. Ryu, J.-W. Park, H.-S. Kim, Ultra-millisecond flip-chip bonding process via intense pulsed light irradiation, ACS Applied Materials & Interfaces 17 (27) (2025) 39694–39707.
[19] J.-H. Jang, C.-J. Lee, B.-U. Hwang, K.D. Min, J.-H. Kim, S.-B. Jung, Microstructural evolution and mechanical properties of SAC305 with the intense pulsed light soldering process under high-temperature storage test, 2021 IEEE 71st electronic components and technology conference (ECTC), IEEE, 2021, pp. 2314-2319.
[20] E. Ha, K.D. Min, S. Lee, J.-S. Hwang, T. Kang, S.-B. Jung, Intense Pulsed Light Soldering of Sn–3.0 Ag–0.5 Cu Ball Grid Array Component on Au/Pd (P)/Ni (P) Surface-Finished Printed Circuit Board and Its Drop Impact Reliability, Advanced Engineering Materials 25 (10) (2023) 2201635.
[21] K.D. Min, E. Ha, S. Lee, J.-S. Hwang, T. Kang, J. Joo, S.-B. Jung, Proposal of intense pulsed light soldering process for improving the drop impact reliability of Sn–3.0 Ag–0.5 Cu ball grid array package, Journal of manufacturing processes 98 (2023) 19–28.
[22] Z.-Q. Zhou, F. Hu, W.-J. Zhou, H.-Y. Chen, L. Ma, C. Zhang, M. Lu, An investigation on a crystalline-silicon solar cell with black silicon layer at the rear, Nanoscale research letters 12 (1) (2017) 623.
[23] M.A. Green, M.J. Keevers, Optical properties of intrinsic silicon at 300 K, Progress in Photovoltaics: Research and Applications 3 (3) (1995) 189–192.
[24] M.A. Green, Self-consistent optical parameters of intrinsic silicon at 300 K including temperature coefficients, Solar Energy Materials and Solar Cells 92 (11) (2008) 1305–1310.
[25] Y.-R. Jang, S.-J. Joo, J.-H. Chu, H.-J. Uhm, J.-W. Park, C.-H. Ryu, M.-H. Yu, H.-S. Kim, A review on intense pulsed light sintering technologies for conductive

electrodes in printed electronics, International Journal of Precision Engineering and Manufacturing-Green Technology 8 (1) (2021) 327–363.
[26] B. Sopori, W. Chen, J. Madjdpour, N. Ravindra, Calculation of emissivity of Si wafers, Journal of Electronic Materials 28 (12) (1999) 1385–1389.
[27] X. Lu, T. Shi, Q. Xia, G. Liao, Thermal conduction analysis and characterization of solder bumps in flip chip package, Applied Thermal Engineering 36 (2012) 181–187.
[28] S. Cho, J.Y. Lee, Heat dissipation of printed circuit board by the high thermal conductivity of photo-imageable solder resist, Electronic materials letters 6 (4) (2010) 167–172.
[29] N. Chowdhury, J. Sun, D.G. Cahill, Anisotropic thermal conductivity of kapton films, composites, and laminates, ACS Applied Polymer Materials 7 (3) (2025) 1440–1447.
[30] P. Rajaguru, H. Lu, C. Bailey, J. Ortiz-Gonzalez, O. Alatise, Evaluation of the impact of the physical dimensions and material of the semiconductor chip on the reliability of Sn3. 5Ag solder interconnect in power electronic module: A finite element analysis perspective, Microelectronics Reliability 68 (2017) 77–85.
[31] Y. Wu, K.-L. Lin, B. Salam, Specific heat capacities of Sn-Zn-based solders and Sn-Ag-Cu solders measured using differential scanning calorimetry, Journal of Electronic Materials 38 (2) (2009) 227–230.
[32] Y. Dou, J. Luo, L. Qi, H. Lian, J. Huang, Drop-on-demand printing of recyclable circuits by partially embedding molten metal droplets in plastic substrates, Journal of Materials Processing Technology 297 (2021) 117268.
[33] D. Liu, J. Yu, Otsu method and K-means, 2009 Ninth International conference on hybrid intelligent systems, IEEE, 2009, pp. 344-349.
[34] H. Qi, N.M. Vichare, M.H. Azarian, M. Pecht, Analysis of solder joint failure criteria and measurement techniques in the qualification of electronic products, IEEE Transactions on Components and packaging Technologies 31 (2) (2008) 469–477.
[35] R. Ghaffarian, Area array technology for high reliability applications, Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging, Springer2006, pp. A283-A312.
[36] J. Feng, D.E. Xu, Y. Tian, M. Mayer, SAC305 solder reflow: Identification of melting and solidification using in-process resistance monitoring, IEEE Transactions on Components, Packaging and Manufacturing Technology 9 (8) (2019) 1623–1631.
[37] M. Harada, R. Satoh, Mechanical characteristics of 96.5 Sn/3.5 Ag solder in microbonding, IEEE Transactions on Components, Hybrids, and Manufacturing Technology 13 (4) (2002) 736–742.
[38] L. Qu, N. Zhao, H. Ma, H. Zhao, M. Huang, In situ study on the effect of thermomigration on intermetallic compounds growth in liquid-solid interfacial reaction, Journal of Applied Physics 115 (20) (2014).
[39] N. Zhao, Y. Zhong, M. Huang, H. Ma, W. Dong, Growth kinetics of Cu6Sn5 intermetallic compound at liquid-solid interfaces in Cu/Sn/Cu interconnects under temperature gradient, Scientific reports 5 (1) (2015) 13491.
[40] M.M. Salleh, S. McDonald, H. Yasuda, A. Sugiyama, K. Nogita, Rapid Cu6Sn5 growth at liquid Sn/solid Cu interfaces, Scripta Materialia 100 (2015) 17–20.
[41] X. Hu, T. Xu, X. Jiang, Y. Li, Y. Liu, Z. Min, Effects of post-reflow cooling rate and thermal aging on growth behavior of interfacial intermetallic compound between SAC305 solder and Cu substrate, Applied Physics A 122 (4) (2016) 278.
[42] M. Yang, H. Ji, S. Wang, Y.-H. Ko, C.-W. Lee, J. Wu, M. Li, Effects of Ag content on the interfacial reactions between liquid Sn–Ag–Cu solders and Cu substrates during soldering, Journal of Alloys and Compounds 679 (2016) 18–25.
[43] M.M. Salleh, C. Gourlay, J. Xian, S. Belyakov, H. Yasuda, S. McDonald, K. Nogita, In situ imaging of microstructure formation in electronic interconnections, Scientific reports 7 (1) (2017) 40010.
[44] A. Paul, T. Laurila, V. Vuorinen, S.V. Divinski, Thermodynamics, Diffusion and the Kirkendall Effect in Solids, Springer, Cham, 2014.
[45] D. Kim, J.-H. Chang, J. Park, J.J. Pak, Formation and behavior of Kirkendall voids within intermetallic layers of solder joints, Journal of Materials Science: Materials in Electronics 22 (7) (2011) 703–716.
[46] W. Wu, H. Yang, Y. Li, Z. Fan, J. Li, Effect of IMC thickness on the mechanical properties of microbumps, IEEE Transactions on Components, Packaging and Manufacturing Technology 13 (2) (2023) 265–273.
[47] H. Liu, C. Xu, X. Liu, D. Yu, F. Dai, Y. Lu, D. Shangguan, Effect of IMC Growth on thermal cycling reliability of micro solder bumps, 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), IEEE, 2013, pp. 836-839.
[48] S. Chen, C. Tsai, N. Kao, E. Wu, Mechanical behavior of flip chip packages under thermal loading, Proceedings Electronic Components and Technology, 2005. ECTC'05., IEEE, 2005, pp. 1677-1682.
[49] C. Burch, K. Vasoya, STABLCOR Groundbreaking PCB and Substrate Material, Special Feature VMEbus Systems Magazine (2005) 56–59.
[50] J. Kinast, E. Hilpert, R.-R. Rohloff, A. Gebhardt, A. Tünnermann, Thermal expansion coefficient analyses of electroless nickel with varying phosphorous concentrations, Surface and Coatings Technology 259 (2014) 500–503.